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COLOR HEAD DOWN DISPLAY PROGRAM

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13. ABSTRACT *(Maximum 200 words)*

The purpose of the CHDD program was to develop a large-area AMLCD for cockpit applications. A 4- x 8-in. polysilicon AMLCD with 320,000 display cells was designed with integrated scanners and fabricated. A support electronics system was constructed that accepted multisource RGB video. This system reformatted the video information to drive the display at 180 fields/second and synchronized the display to a color sequential backlight. Moving the color information into the temporal domain, maintained the color pixel density identical to the cell density.

A 192 x 192 pixel active matrix circuit with integrated drive and scan functions was fabricated in thin-film single-crystal silicon, using standard IC processing, and subsequently placed on glass to form a transmissive AMLCD. The first assembled 2.5- x 2.5-in. monochrome display shows greater than 85 percent pixel functionality. The speed, low leakage current, and high drive capability of single-crystal silicon devices should allow the fabrication of displays with integrated system-level peripheral circuitry, high pixel density, and improved contrast and optical aperature ratios.

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PREFACE

The completion of the Color Head Down Display program depended on the cooperation of a number of individuals at the David Sarnoff Research Center (Sarnoff). TFT active matrix and integrated CMOS scanner design, fabrication, device characterization, and electrical testing activities were capably handled by Alfred C. Ipri, Dilip K. Pancholy, David A. Furst, S. N. Lee, Jeff Via, Grzegorz Kaganowicz, Brian W. Faughnan, and John Valochovic. Frank P. Cuomo and Thomas L. Glock skillfully assembled, filled, and sealed some of the early finished display devices. David L. Jose established the system architecture and design for the video interface electronics and color-sequential backlight. The system integration, board layout, and construction, was coordinated by Jacob P. Hasili.

The silicon transfer programs depended on the cooperation and technical assistance of N. Cheong, D. Leber, S. Leary, and R. Morrison at Kopin and J. Valachovic, F. Cuomo, J. Hasili, and J. Via at Sarnoff. The insight and support provided by Dr. J. Fan and Mr. J. Jacobsen is also gratefully acknowledged. This work was supported by the Defense Advanced Research Projects Agency through Wright Laboratory, Wright Patterson Air Force Base.

Program Manager was Roger G. Stewart; Al Ipri and David Jose were the Principal Investigators for the two parts of this contract. The contract was monitored initially by John Coonrod and later by Robert Michaels of the Cockpit Directorate (AFWAL/KTD), whose support and advice were very helpful.

1. CHDD SUMMARY

The primary goal of this contract was to produce a large-area polysilicon active matrix liquid crystal display (AMLCD).

Over the past 4 years of this contract, the cost of polysilicon AMLCD plate processing has required a 3 million dollar capital expenditure and 8 million dollars in operating costs. Thirty percent of this operating cost was funded under this contract, and 70 percent was covered by commercial customers and Sarnoff internal funding. During this period, we have had fewer than 12 full-time support staff supporting this effort and an expenditure rate of 2 million dollars a year.

We have learned from this experience, that a successful AMLCD fabrication facility will require a 20 to 100-million dollar investment, 50 to 100 full-time staff, and an expenditure rate of 5 to 10 million a year to maintain a constant throughput from the facility.

The inability to produce a fully functional, defect-free Color Head Down Display also indicates that it is better to have a simplified display design rather than rely upon redundancy to overcome the defects.

There were three remaining problems with the color-sequential grayscale display system:

First, the reduced contrast ratio of 17:1 was primarily influenced by pixel leakage and the combined disclinations and boundary effects in each cell.

Second, the color of the color-sequential system is desaturated due to phosphor emission persistence of the backlight lamps, the delay in the liquid crystal response, the aforementioned reduced contrast ratio, and the charge redistribution of the pixel capacitance as it is sequenced through the three different color fields.

The third problem is the image artifacts due to the variability of the demultiplexing of the input data.

2. INTRODUCTION AND ACCOMPLISHMENTS

2.1. BACKGROUND

The David Sarnoff Research Center (Sarnoff) has played a significant historical role in the development of flat displays. The original discovery of electro-optical effects in liquid crystal materials at Sarnoff[1] led to the first liquid crystal display (LCD).[2] Pioneering work on matrix-addressed displays,[3] as well as research on thin-film transistors (TFTs),[4] was performed here; in addition, large flat cathode-ray tubes (CRTs) for wall TV applications have been extensively studied.[5,6] Present efforts are aimed at developing active-matrix TFT LCDs for high-resolution, full-color, flat, analog displays.

Sarnoff has emphasized the development of polycrystalline silicon (poly-Si) TFTs deposited on relatively inexpensive glass substrates for its active-matrix LCD program. No other active-matrix technology has all the critical virtues of high mobility, good stability, relatively inexpensive (glass) substrate, CMOS, and high-quality interconnects. We have also developed on-plate integrated scanner circuits to eliminate the large number of intrinsically unreliable connections to the row and column lines of the display from external matrix-addressing drivers. Scanned display devices for the present CHDD contract consist of a 400 x 800 TFT array with an element pitch of 0.250 mm (100 lines/in.). The integral CMOS scanners have 5-bit-wide data channels, with integrated chopped ramp digital-to-analog converters.

2.2. COLOR HEAD DOWN DISPLAY SYSTEM CONCEPT

In the Sarnoff scanned displays, the twisted-nematic liquid crystal (TNLC) cells act as light valves to modulate the transmitted light from an illuminator. The basic cells exhibit an analog transfer characteristic, which produces a continuous, monotonically decreasing brightness for the given picture element in response to a continuous, monotonically increasing video signal. The poly-Si TFT scanners developed by Sarnoff have a speed capability higher than is needed for display frame rates of 60 Hz.

The need for brighter and more efficient military displays has led to the concept of a color-sequential fluorescent backlight for the illumination of a large-area LCD. In a field-sequential color system, video information for each primary color is loaded into the liquid crystal array, one complete color field at a time. The liquid crystal cells will synchronously modulate the light from a corresponding temporally sequenced three-color light source. With a high enough sequencing rate, a viewer will see a full color image with a color gamut that is limited by the chromaticity coordinates of the three color light sources. There will be no light attenuation resulting from the

presence of a filter, and each picture element corresponds to a single liquid crystal cell instead of a group of three or more cells that form a color filter pixel. This display will, therefore, have much higher brightness and resolution than a color filter LCD for a given power input and display size.

2.3. ACCOMPLISHMENTS

Under the Color Head Down Display portion of this contract, Sarnoff has designed, constructed, and demonstrated a large-area LCD with an analog video interface system color-sequential backlight system. The milestones in the course of this work, have been:

- The development of an integrated functional test and repair station
- The completion of the support electronics system (SES)
- The integration of the color-sequential backlight system
- The selection of either the silicide or double metal option for faster display operation
- The selection of internal or external display assembly locations
- The fabrication and assembly of a 4-x 8-in plate that operates at 180-Hz field rate
- The integration of the display, color-sequential backlight, and SES for final demonstration.

Other accomplishments under this part of the contract have been the:

(1) Demonstration of 192 x 192 displays with 0.1-in flush seal edges

(2) First demonstration of the color-sequential backlight system

(3) LAF start-up and first successful stepper assembly of a complex circuit

(4) Successful completion of the 4-x 8-in grayscale display design

(5) Fabrication of CHDD with functioning data/select scanners

(6) Fabrication of the first 4-x 8-in display with integral black matrix

(7) Automatic testing and yield data base

(8) Automatic testing and yield data base

(9) Line, parametric, and WAT yields over 70 percent

(10) Low resistance gates (Rho = 0.25 Ω/q)

(11) Low resistance N+ source/drain regions (Rho = 350 Ω/q)

(12) Combined functional test and repair station

(13) Fabrication and assembly of 4-x 8-in plate that operates at 180-Hz field rate

(14) Generation of 11 patent disclosures

3. DISPLAY DESIGN

3.1. GENERAL

Integration of the scanning circuitry needed to drive the 400 x 800 pixel AMLCD was achieved by fabricating both data-line and select-line driver circuits on the 127-mm x 228.6-mm rectangular glass substrate along with the same polysilicon thin-film pixel transistors used to improve the optical performance of the display. The maximum processing temperature in the polysilicon transistor fabrication process is kept below 650°C to prevent melting or warpage of the low-cost glass substrates.

Since the display IC is too large to fit within the field of even a 2:1 wafer stepper, the 125-x 225-mm design must first be preassembled on a CAD workstation and then partitioned into 17 smaller reticle segments. These segments were MEBES written onto a 7-in reticle as shown on Fig. 1. The final assembly of the display was completed by programming a large-area wafer stepper as shown in Fig. 2.

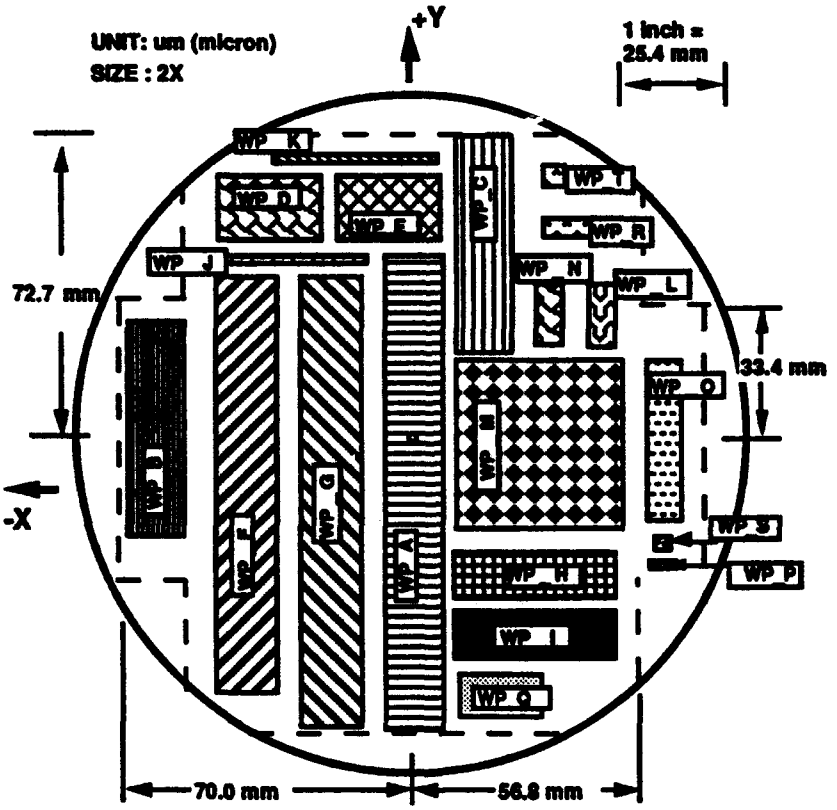


Figure 1. *Reticle Layout.*

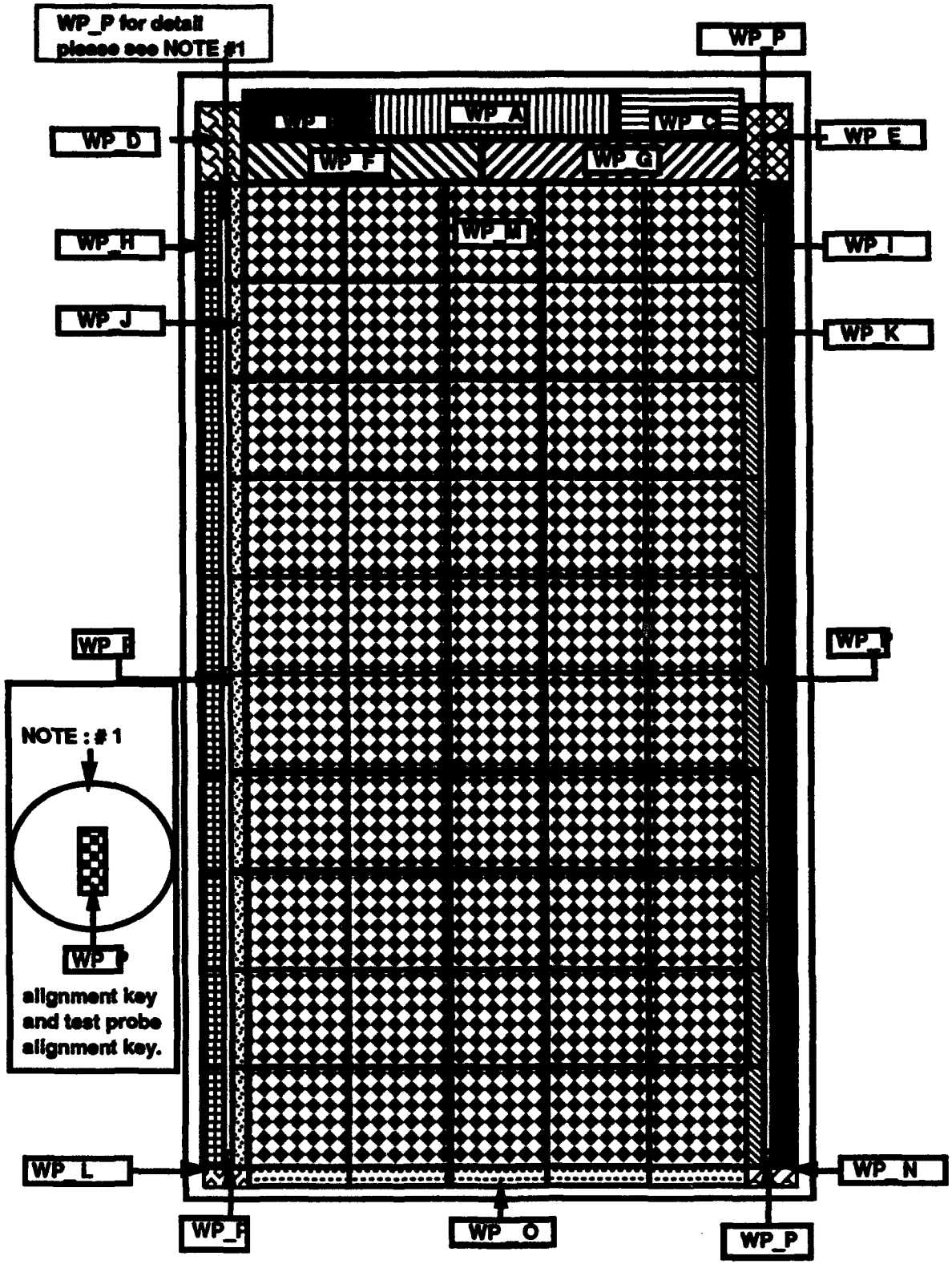


Figure 2. *Reticle Segmentation Diagram.*

3.2. DISPLAY CIRCUIT OPERATION

The scanner circuits are implemented in dynamic CMOS circuitry. A single-data scanner is located at the top of array, as shown in Fig. 3. The select scanners are on the left and right. The circuitry is divided into 54 independent blocks to increase the effectiveness of the redundancy and laser repair procedures. There are 25 blocks of 4 data line scanners plus 4 separate circuit blocks for the select scanners.

Figure 4 shows the circuit block diagram for the integrated scanner display. The diagram, also shows the "Chop Ramp" scanning technique that is used to handle the 32 gray levels color display requirement. Each data line is driven by a transmission gate controlled by the output of a 5-bit counter. During the first line period, the 5-bit grayscale code for each pixel is loaded into the data shift registers. At the end of the line period, the data are transferred (2000 bits at a time) from the shift register latches to the counters. A control-latch flip-flop is also reset to turn on all 400 transmission gates. During the second line period, the master data bus is ramped by a low impedance driver from 0 V to 5 V.

The master data line ramp is always the same and no longer contains any information. The analog voltage presented to the data lines now depends entirely on the contents of their respective counters. After a short delay, the counter clock starts incrementing all of 800 data line counters. Whenever each counter reaches count of 11111, it sets the control-latch flip-flop to turn off the transmission gate. For example, if a 11111 code is loaded into data line No. 118, then its transmission gate will remain conducting only long enough to discharge its data line completely to ground. At the same time, if data line No. 122 is loaded with a 00000 code then its transmission gate will remain conducting throughout the entire line period, allowing its data line to become fully charged to the 5-V level. Data lines with intermediate binary codes, such as line No. 120, will be charged to intermediate levels before their transmission gates turn off and chop or "freeze" that particular data line at an intermediate point on the ramp. This "Chop Ramp" scanning circuit achieves an accurate, uniform, 32-step digital-to-analog conversion.

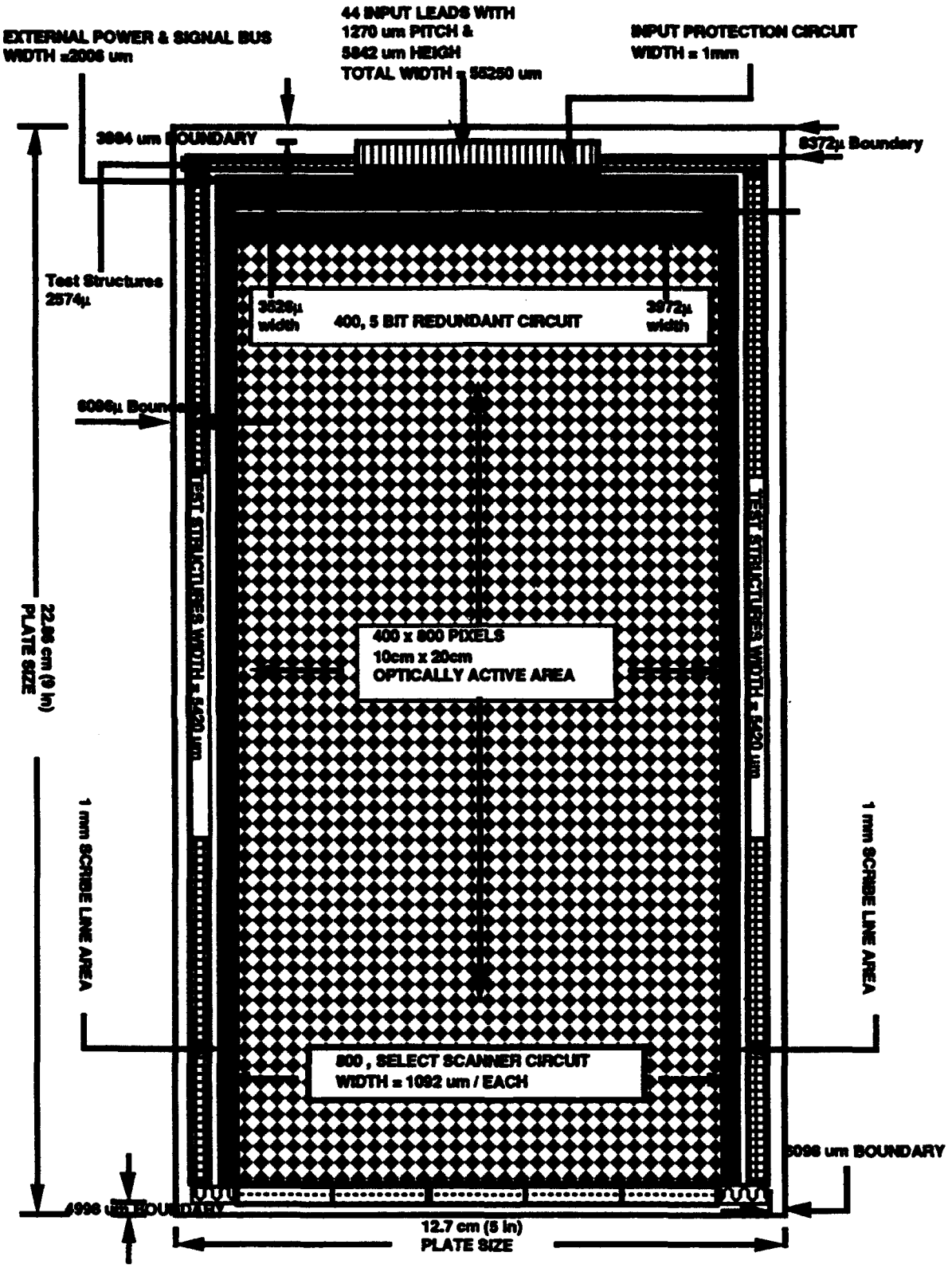


Figure 3. *CHDD Layout.*

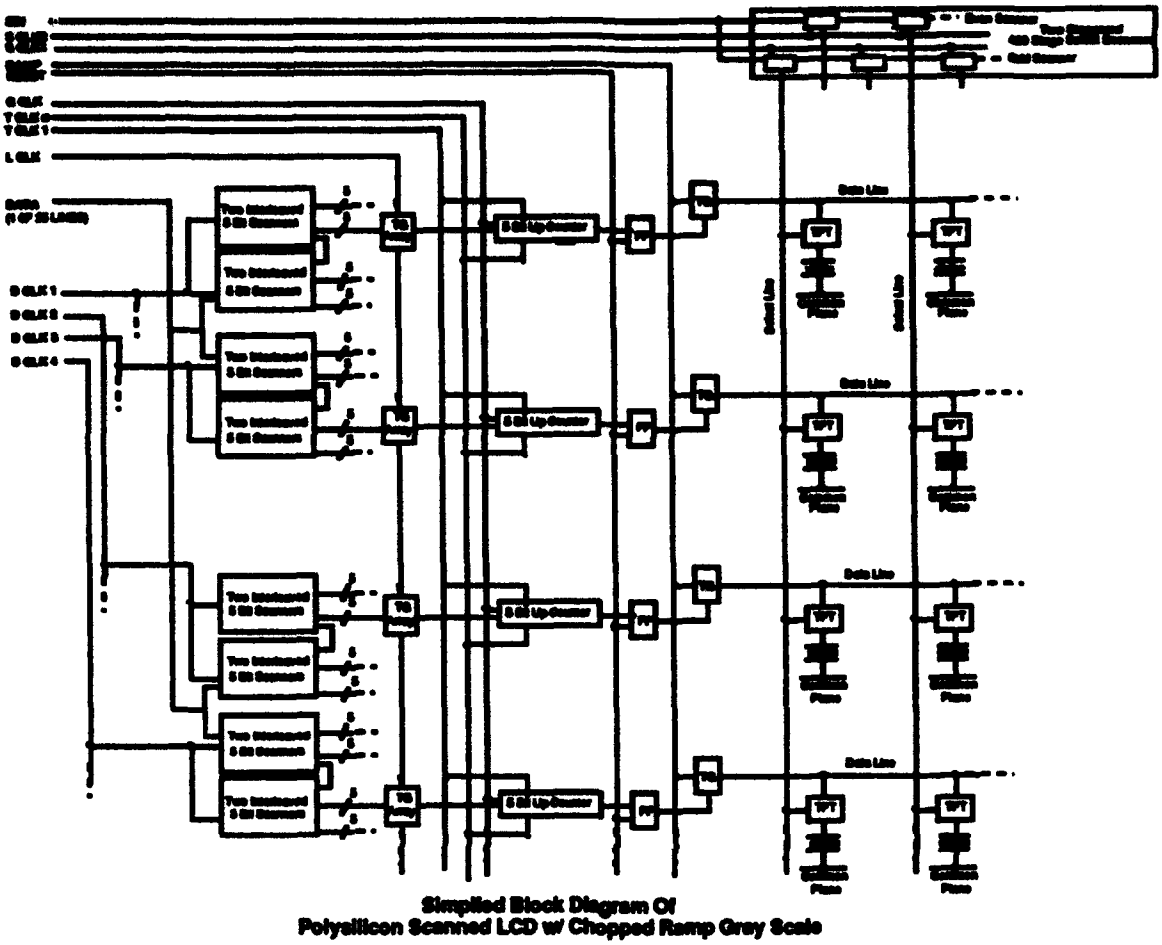


Figure 4. *CHDD Simplified Block Diagram.*

3.3. DATA SCANNER

Figure 5 shows the circuit for one stage of the data scanners. These data scanners are partitioned into 100, 4 x 5 serial-loaded registers driven from a reformatted 4:1 multiplexed 25-line-parallel-bus running at 8 MHz. Each of the 25 leads is connected to the inputs of four, 20-stage shift registers. These four shift registers are driven by four external clocks that are separated by 90°.

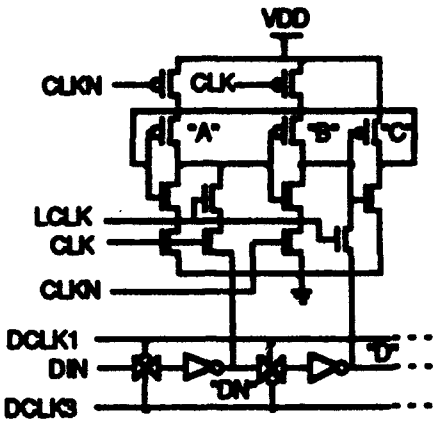


Figure 5. *Data Scanner Single Stage Schematic.*

3.4. SELECT SCANNER

An improved voltage level shifter circuit was designed for the select scanner circuit. A conventional level shifter circuit will not always function properly with certain poor device characteristics and high operating voltages. As shown in Fig. 6, N1 and N2 form a current mirror. When Vin = 0 V, P1 is off, P2 is on, and N1 conducts no current. With no conducting current mirrored in N2, node "b" will be pulled up to 15 V by P2. When Vin = 15 V, P1 is on, P2 is off, the N1 current will be mirrored into N2, and N2 will drain the current at node "b" until the node reaches -5 V.

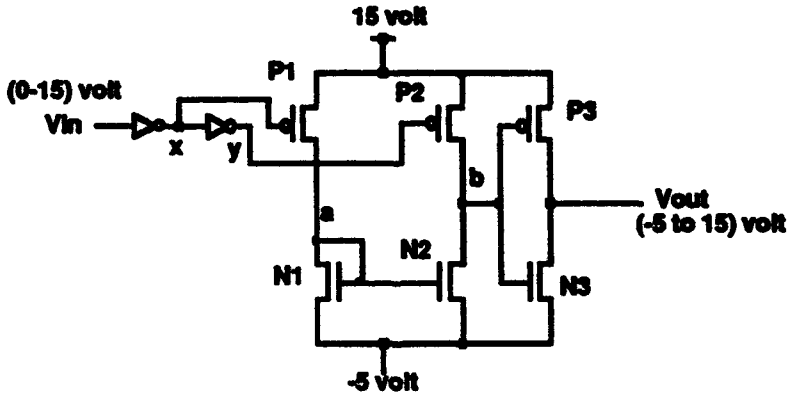


Figure 6. *Level Shifter Schematic.*

3.5. D/A CONVERSION

In order to achieve the video rate operation, a high-speed grayscale counter is required. Figure 7 shows the first stage frequency divider circuit for this grayscale counter. By introducing

the signal TCLK, the feedback path used in the typical frequency divider circuit is not required. This frequency divider circuit can be operated up to 6 MHz despite the limited 10 cm^2/V-sec polysilicon transistor mobility.

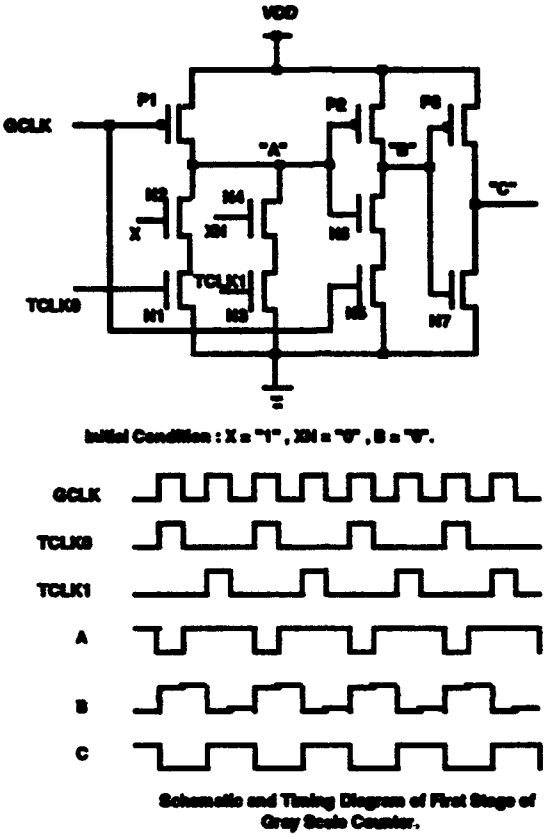


Figure 7. *First Stage Grayscale Counter Schematic.*

The integration of the scanning circuitry on the 127-mm x 228.6-mm plate has reduced the number of input leads from 1200 to 44 and dramatically illustrates the potential of wafer scale integration techniques to improve reliability and reduce cost.

4. PROCESSING

4.1. PROCESS FLOW

Nine-inch-diagonal LCDs with integral scanners were produced on 5-x 9-in rectangular glass substrates. Both the data-line and select-line drivers circuits were fabricated simultaneously on a 250-μm pitch. The picture element (pixel) array was comprised of 400 x 800 pixels containing polysilicon thin-film transistors as the switching elements. The process used to fabricate the transistor array is described below.

The process flow for the fabrication of the 400 x 800 transistor array is shown in Fig. 8. The starting glass material was Hoya NA-40, which has a maximum processing temperature of 650°C. In order to use the glass at this temperature, however, it is necessary to anneal it at various temperatures and times to "stabilize" the glass so that subsequent high-temperature processing steps will not cause movement in the glass of > 50 ppm. The photolithographic aligner that is used in this process is capable of magnification compensation of about 70 ppm and, hence, it is desirable to keep the glass movement below this maximum value. After glass anneal and cleaning, the first silicon layer (1500 Å) is deposited at a temperature of about 560°C. At this temperature, the deposited silicon layer is essentially amorphous with small grains located at the glass-silicon interface. These grains serve as nucleation sites for subsequent grain growth during later high-temperature steps.

After removal of the silicon from the display back surface, the front surface silicon layer is photolithographically patterned and etched to form transistor islands. Next, a 750-Å gate oxide is grown at approximately 640°C. During this oxidation step, the silicon film is completely recrystallized to form a continuous layer of grains that are approximately 100 to 300 nm across. This recrystallization process is important in forming relatively large grains that produce carrier mobilities in the 15-30 cm^2/V-s range. After the gate oxide is grown, the second silicon layer (5000 Å) is deposited and doped by ion implantation. This layer is then patterned to form the gates of the transistors and any low resistance crossovers needed in the circuit.

Phosphorous and boron implantations are used to form the self-aligned source/drain regions, and the implants are activated by a 640°C oxidation step. This step is also used to convert the gate silicon to polysilicon and to form an oxide over the polysilicon gate material. A thick (8000 Å) oxide layer is then deposited over the surface of the plate, and contact vias are etched in the oxides to permit access to the underlying silicon layers. A 1 μm of aluminum is then deposited over the surface and patterned to form the interconnect layer and silicon nitride is deposited. During the silicon-aluminum alloy step the polysilicon transistors are hydrogenated in order to

reduce the effects of the silicon grain boundaries and permit lower leakage (off) currents. Openings are cut in the nitride layer to allow electrical connection and the array is complete.

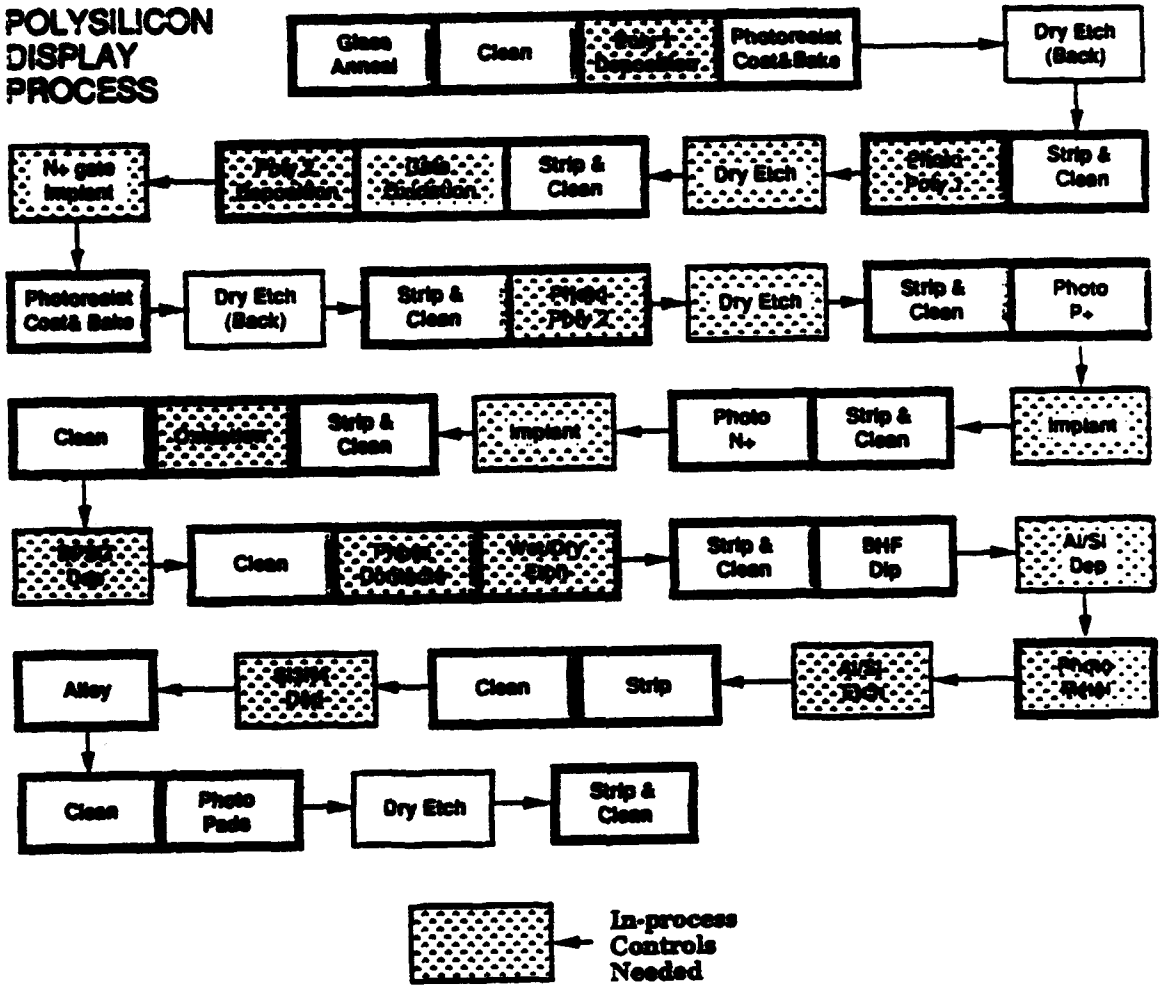


Figure 8. *Polysilicon Process Flow Diagram.*

In order to form a liquid crystal array, the polysilicon arrays are shipped to Standish Industries for assembly. They apply an alignment layer to the surface of the polysilicon plates and "rub" the surface to form small microscopic striations that permit alignment of the large liquid

crystal molecules. A top plate is then attached to the polysilicon plate and the region between the two plates is filled with liquid crystal material. After sealing of the fill port, the liquid crystal assembly is complete and the display is ready to light up!

4.2. FABRICATION AND TEST EQUIPMENT UPGRADES

In this section, the equipment and process upgrades that have been implemented since the start of the LCD Program in order to achieve the goal of increased yield and improved manufacturability are listed, and the expected effect on yield of these changes is provided. Actual yield results will be treated in Section 4.

1. TFT Fabrication Equipment Upgrades

The major equipment upgrades implemented during the course of this program are listed below:

(1) Installation of spin developer

(2) Installation of class 10 photoresist bake oven

(3) Improvement of HEPAs over the silicon etcher

(4) Upgrading of cleanroom:

  (a) Install 16 new HEPA filter assemblies

  (b) Increase area of 16 return air ducts

  (c) Enlarged changing area

(5) Conversion of cleaning baths to 100 percent quartz for exposed areas.

2. TFT Fabrication Process Changes

The major equipment process changes implemented since the start of this program are listed below:

(1) Implementation of routine cleaning of the oxidation furnace

(2) Implementation of routine SIMS and SPV measurements to monitor Si and SiO_2 quality

(3) Utilization of full bunny suits

(4) Change in procedure to allow only one person in the photoroom during photoresist application.

3. Test, Repair, and Assembly Upgrades

A new laser repair system was installed that allows us to laser repair defects in the same test bed that is used to measure plates and locate defects. This has lead to an approximate three-fold reduction in time taken for laser repair. No major changes were implemented in the assembly of LCDs.

4.3. POLYSILICON PROCESS YIELD CHARACTERISTICS

1. Yield Model

A model has been previously developed for predicting the yields of display plates. The input to this model is an estimate of the defect level achieved on display plates processed in our LAF. Each of these plates includes test structures for measuring opens (serpentine) and shorts (interdigitated). These test structures are located on the periphery of the plate. Since this region usually suffers from a higher level of defects than central locations, these devices provide a worst-case estimate. Test structures exist for: active polysilicon, gate polysilicon, and aluminum levels. The polysilicon design rules are 6-μm lines and spaces, and the aluminum design rules are 8-μm lines and spaces. The structures comprise a linear distance of 3.2 m. In addition, a string of 83,200 6-x 6 μm contacts, in series with the active polysilicon level, and another string in series with the gate polysilicon levels, are monitored.

For active-matrix arrays and integrated drivers, a linear yield model is appropriate, i.e., the probability of finding a defect is proportional to the length of certain critical lines. This is true for both opens and shorts. Shorts will occur between parallel lines of length, L, and spacing, d. The longer the line and the closer the spacing, the more likely the short will occur. This is in contrast to some yield models for integrated circuit chips, where the probability of defects occurring is proportional to the area of the chip.

If the probability of a defect occurring is proportional to the length, and this probability is D_0 per unit length, then it is easy to show that the yield for a line of length L is:

$$Y = \exp\text{-}(D_0 L) \qquad (1)$$

We obtain the value of D_0 experimentally from the test structures of length L_t, which have measured yield Y_t, i.e.,

$$Y_t = \exp\text{-}(D_o L_t) \tag{2}$$

The same yield model can be adapted to predict yields for redundant structures. For example, consider the case of redundant data lines, i.e., every data line is driven separately from each side of the array. It then takes two defects in one line to produce a line defect, since for one defect, the line segment on either side of the defect will be driven by its own driver.

From Eq. (1), the probability of obtaining a single defect on a particular data line is:

$$P_d = 1 - \exp\text{-}(D_o L_d) \tag{3}$$

where L_d is the length of a single data line. This expression is actually the probability that a data line has any number of defects, but will be almost equal to the single-defect probability for small $D_o L_t$. Now the probability that a particular data line, which is known to have one defect, has a second defect, is simply the product P_d^2. This follows from the assumption of statistical independence. Therefore, the yield for a redundant data line is:

$$Y_d = \left[1 - \left(1 - \exp\text{-}(D_o L_d)\right)^2\right] \tag{4}$$

and the redundant yield for the entire array of N_d data lines is:

$$Y_d = \left[1 - \left(1 - \exp\text{-}(D_o L_d)\right)^2\right]^{N_d} \tag{5}$$

If $D_o L_d \ll 1$, $\exp\text{-}(D_o L_d) \approx 1 - D_o L_d$, and:

$$Y_d = \left[1 - (D_o L_d)^2\right]^{N_d} \approx 1 - N_d * (D_o L_d)^2 \tag{6}$$

In order to calculate yield, the display plate is separated into several key areas including:

(1) General busing

(2) Data scanners, including central and side busing

(3) Select scanners, taking driver redundancy into account

(4) Select to data shorts

(5) Data line opens.

Lines and spaces with critical dimensions were identified for the aluminum, active polysilicon, and gate polysilicon levels, and their lengths and widths were measured. Non-design-rule sized widths are given a linear weighting when calculating their effective length. For instance, a 14-μm-wide aluminum line of 1 m in length would be treated as the equivalent of an 8/14-x 1-m-long line, or 0.57 m in effective length.

2. Yield Data for TFT Process

Applying the yield model to the yield data that we have been continuously monitoring for aluminum, active polysilicon, and gate polysilicon levels, enables us to measure the effect of improvements in the process. The following graphs, which are ordered chronologically, illustrate our progress. All of the yield calculations are based on test structures measuring opens and shorts yields for a given level. No provision has been made in our model to account for inter-level shorts. We believe such shorts are insignificant compared with shorts within levels.

Figure 9 shows the aluminum-level yields for the opens and shorts structures on actual TFT plates, averaged by lot, and plotted as a five-lot moving average. When there is a high level of shorts, the opens structures are less likely to fail, due to internal shorts in the serpentines, and when there is a high level of opens, due to aluminum corrosion, for instance, the shorts structures are less likely to fail, due to a high level of internal opens. The product of the two yields helps balance out these effects, and hence, is a more reliable number, or figure of merit. Figure 9 shows that we have been successful at improving the aluminum yields; the figure of merit went from a high of 39 percent prior to 12/90 to a high of 62 percent on these five-lot moving averages.

Aluminum opens were improved by altering the etching process to avoid over-etching, hardening the photoresist, and rapidly removing the chlorine-laden resist after the etching process, by immersion in RT2, to arrest corrosion. Aluminum shorts were reduced by mounting the plates upside down during etching, paying careful attention to polymer build-up in the aluminum etcher, adding a spin developer, changing personnel procedures, and upgrading the air handling in our facility.

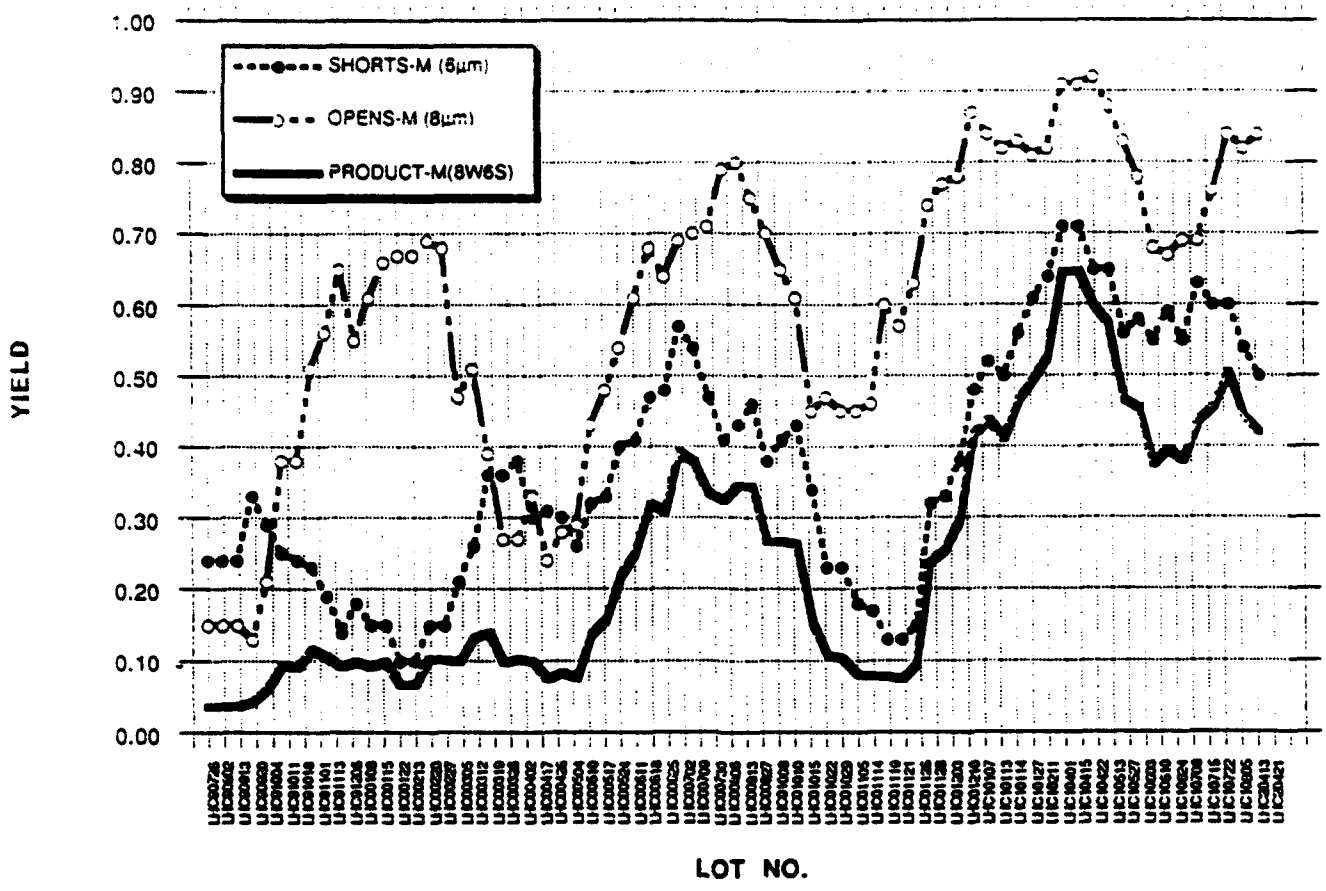


Figure 9. *Five -Lot Moving Average of aAluminum Shorts and Opens Yield Data.*

The following yield structure table, Table 1, illustrates the benefits produced by improvements to our facility. The opens structure yield was greatly improved by the introduction of spin development. The shorts structure yield has steadily improved by both implementing spin development and upgrading the procedures and air handling in our facility.

TABLE 1. Tabulation Of Yield Improvement Due To Facility Upgrades

	Prior to spin development implementation (prior to 12/91)	After spin development implementation (4/92)	After spin development plus general facility upgrade (8/92)
Opens Yield	82 ± 16%	98 ± 1%	97 ± 3%
Shorts Yield	55 ± 16%	72 ± 20%	86 ± 6%

The yield results for opens and shorts and their product for the active polysilicon level are shown in Fig. 10. This graph shows essentially no improvement in the active polysilicon level yield; however, the effects of our upgrade of our facilities has not entered the data base. The data is once again shown as a five-lot moving average.

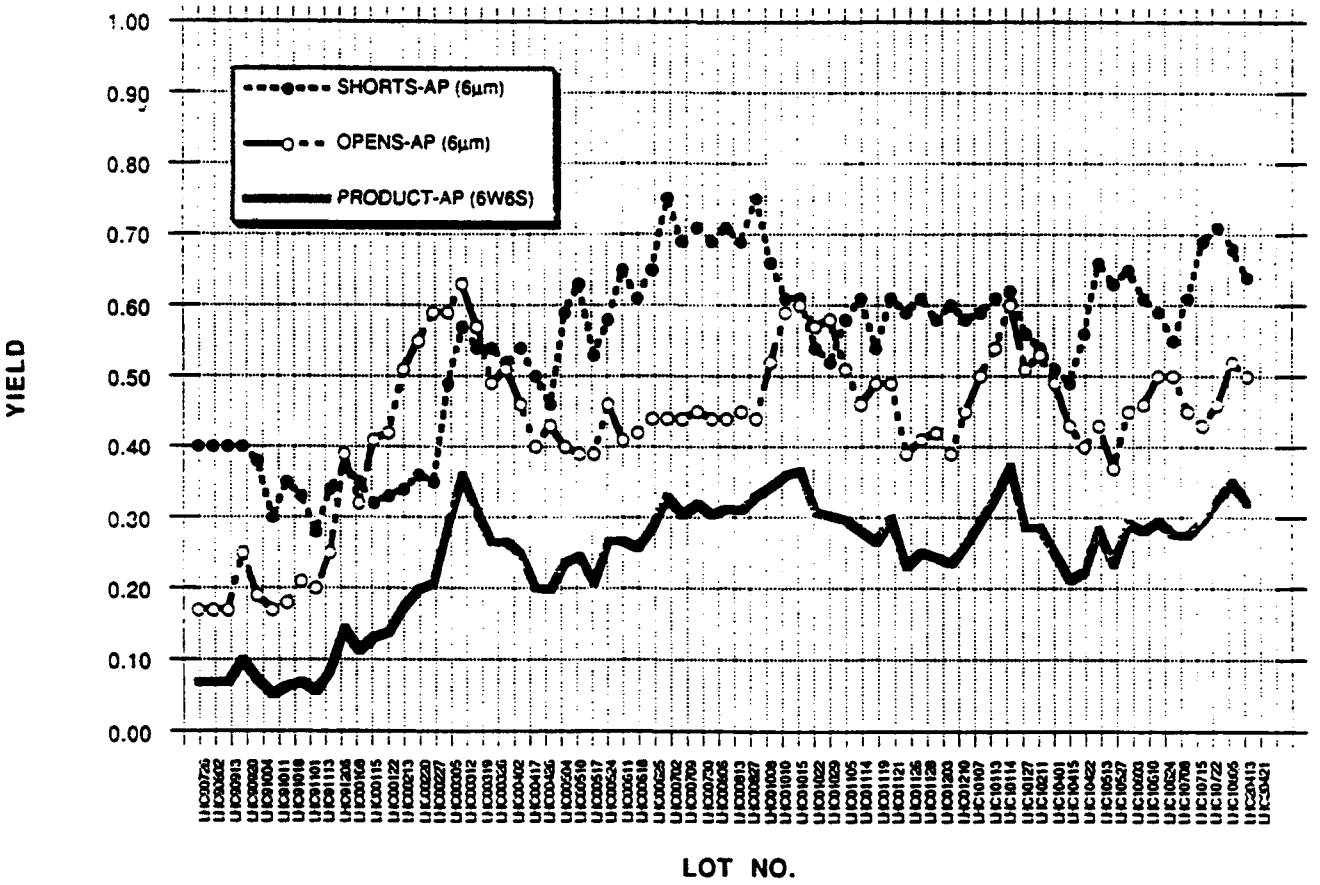


Figure 10. *Five-Lot Moving Average of Active Polysilicon Shorts and Opens Yield Data.*

The gate polysilicon yield results are shown in Fig. 11. This level started off with the highest yield and it has been the most consistent level, particularly with respect to opens. In several lots the yield has been 100 percent for gate polysilicon opens. Like in the case for the active polysilicon level, the effects of our upgrade of our facilities has not entered the data base.

Contact string yields have also been monitored. These test structures do not separate step coverage problems from contact problems. Therefore, loss of yield is not strictly due to contact problems, particularly with respect to gate contacts. At the active-polysilicon level, the test structures suffered from high active polysilicon sheet resistivities, particularly recently, due to contamination of the polysilicon. Improvement in the quality of the polysilicon lowered these resistivities and improved the yield. Contact yield is not separately considered in our yield model, but would obviously be a factor in regions with a high density of contacts, such as the data scanners.

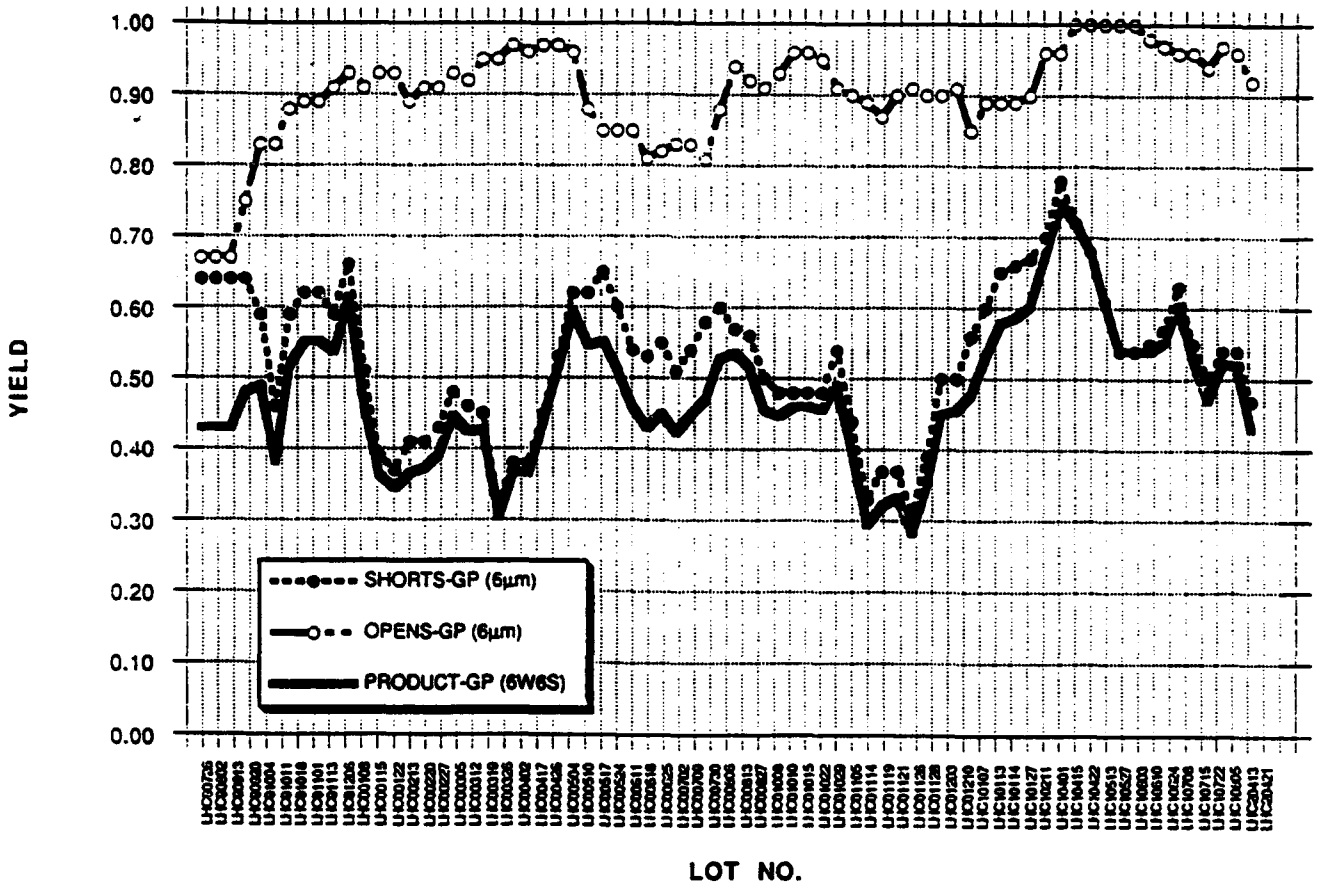


Figure 11. *Five-Lot Moving Average of Gate Polysilicon Shorts and Opens Yield Data.*

In making yield estimates based on test structure yields, for lots started prior to December 1, 1990, we chose the lot with the best product of opens and shorts yields, averaged over a single lot, for that particular level (see Table 2). This estimate shows our status at the start of the LCD Manufacturability Program. A second estimate of yields is calculated using the best data to date (11/15/92). These data were derived from special test plates upon which only one level was patterned. To calculate the effective yield length, L, the display plate has been broken down into various locations: data lines in the array, select scanners, data scanners, general busing, select-to-data shorts, pixel-to-pixel shorts, and pixel source-drain opens. Because there was 100 percent yield of the test structures for gate polysilicon opens in the lots selected, the critical area of the gate lines was not calculated. Furthermore, the yield of the select lines is assumed to be 100 percent. The following lots were selected for the December 1, 1990 estimate, comparing yields for devices similar in size to those on our test plates.

TABLE 2. December 1990 Test Structure Yield

	Opens Yield	Shorts Yield
LHC01128 for the aluminum level	83%	83%
LHC00305 for the active polysilicon level	67%	75%
LHC00504 for the gate polysilicon level	100%	83%

Our best ever yield data on test patterns achieved $y_{open} = 100$ percent, $y_{short} = 94$ percent for aluminum test patterns (plate TSA20904-71), $y_{open} = 99$ percent, $y_{short} = 92$ percent for active polysilicon test patterns (plate TSA20604A-5), and $y_{open} = 98$ percent, $y_{short} = 98$ percent for gate polysilicon (plate TSA20603G-6). However, to be conservative we think that a more realistic yield estimate is as shown Table 3.

TABLE 3. November 1992 Test Structure Yield

	Opens Yield	Shorts Yield
Aluminum level	98%	85%
Active polysilicon level*	98%	85%
Gate polysilicon level*	98%	85%

* These data are what we consistently achieve on aluminum test patterns; the etching performance on active and gate polysilicon should be at least as good.

4.4. YIELD ESTIMATES FOR LAF TFT PLATE FABRICATION

1. Model for Simple Active Matrix Array

By far the most troublesome yield problem for an AM TFT plate is that of open data lines. The yield model in Section 4.3.2 above is used to correlate the data line yield to the test structure yield and the result is plotted above. Note that to achieve interesting yields (above 10 percent) the test structure yield must exceed 91 percent. Based on aluminum etching yields alone, the predicted data line yields for plates processed in 1990 and those processed in 1992 are shown in Table 4 below.

TABLE 4. Measured Yield of Test Structure and Calculated Yield of Data Line Defect Free Displays at the Beginning and End of this Program

	Measured aluminum test structure opens yields	Calculated data line defect-free TFT plate yield
1990	83%	1%
1992	98%	60%

Thus, we can see what dramatic progress has been made during the course of this program.

2. Model of AM Plate Including Integral Scanners

We now proceed with a more complete set of yield calculations for the case of an AM plate that includes integral scanners. In constructing the yield model, we have assumed that defects are random and not caused by improper processing, systematic problems, or mishandling. For the calculations that follow, we have made the following assumptions:

a. Input Busing

Input buses are wide enough that opens are negligible.

The yield loss due to shorts can be estimated from the aluminum test structure yield and the critical area, the gaps between the busing.

Shorts between adjacent buses can be repaired 90 percent of the time.

b. Data Scanners

We estimate the yield of data scanners by assuming that the area of the scanner is occupied by active poly, gate polysilicon, and aluminum in approximately equal amounts, that both shorts

and opens contribute to the yield loss for each, and that the shorts and open yields can be calculated from the test structure yield.

If a data scanner is inoperable, we assume that we can substitute the data from a working data scanner onto the data line originally connected to an inoperable data scanner.

When it is required, such a nearest-neighbor repair is assumed to be successful 80 percent of the time.

c. Select Scanners

The yield is similarly based on the test structure yield of active polysilicon, gate polysilicon, and aluminum.

Only one scanner is required to work all the way to the end so that an inoperable scanner can be cut free 100% percent of the time.

d. Data Lines

The dominant source of nonrepairable yield loss from our original display plate design came from open data lines in the array. As mentioned above, we now can achieve opens yields on aluminum test structures in excess of 98 percent, which translates to data line yields exceeding 60 percent and we would expect this to rise substantially as we move forward.

Although we could do a weld of one data line to its broken neighbor to provide a signal to the disconnected bottom portion of this data line, we do not presently test the display for open data lines and, thus, do not do this repair.

Thus, our model does not assume data line repair.

Yield predictions have been made using the above assumptions with the data collected from the test structures providing the estimates of defect densities for each of the levels. For calculations of the yield of the circuitry, we have used a somewhat more sophisticated model than that described above. The calculations, which are believed to be more accurate over a specific limited range of yields, are based on the Murphy yield model (for $y > 30$ percent) and the Seed model (for $y < 30$ percent).

We report below the results of these calculations assuming either (1) no nearest neighbor substitution of data scanners or (2) nearest neighbor substitution of data scanners, which again is successful 80 percent of the time. In any case, we still assume repair of input busing (90 percent effective), select scanner substitution (100 percent effective), and crossover shorts (also 100 percent effective). This last assumption is only strictly true if either both select scanners are operable or the short can be cleared without cutting a select line. This assumption does not appear to introduce significant error for the level of crossover shorts currently observed.

For the calculations of factory yield we assume that the defect level is proportional to the "class" of the facility. The measured airborne particulate level in our present photolithography facility is typically 50 defects greater than 5 microns in a cubic foot of air. This is 5 times higher than a class 10 facility. Thus, in our factory yield calculations, we have assumed defect densities for all levels that are five times lower than our present (1992) test structure measurements. See Table 5.

The reason these two cases are of interest, is that in the first case each pixel gets exactly correct data, whereas in the second column, the data on one or more columns are repeated to achieve a "line defect free look."

TABLE 5. Calculated Repairable Yields of Data Line Defect Free Displays and of "Nearest Neighbor Data Scanner Substituted" Displays at the Beginning and End of this Program

	TFT plate yield without nearest neighbor data scanner substitution	TFT plate yield assuming nearest neighbor data scanner substitution
1990	3%	14%
1992	7%	27%
Class 10 Factory	43%	59%

3. Model of AM Plate Incorporating Low TFT Count Scanners

We notice that for the existing design when fabricated in our present facility, the yield is reduced from 60 to 27 percent by the incorporation of the present 5-bit data scanners and the relatively complicated 20 TFT select scanners. Newer designs use considerably fewer TFTs. One particular design incorporates as few as 20 TFTs in a data scanner (compared with the 120 per data line in the existing design) and uses only 4 TFTs in the select scanner (compared with the present 20). Such a design would be significantly easier to fabricate. The estimates, again assuming nearest neighbor substitution or no substitution, are shown in Table 6.

TABLE 6. Calculated Repairable Yields of Data Line Defect Free Displays and of "Nearest Neighbor Data Scanner Substituted" Displays for Existing 5-Bit Design and for New Low TFT Count Design

	TFT plate yield without nearest neighbor data scanner substitution	TFT plate yield assuming nearest neighbor data scanner substitution
1992	14%	27%
1992 (low TFT count design)	42%	57%

In this case, the yield loss due to the presence of scanners is almost negligible.

4. Issues Related to Achieving a Line Defect Free TFT Plate from our LAF

a. Silicon Deposition, Etching, and Oxidation

Processes are under control.

b. Ion Implantation

Process is under control.

c. BPSG Deposition and Etching

Processes are under control, although deposition is still somewhat dirty.

d. Aluminum Deposition and Etching

Processes are under control.

e. Nitride Deposition

This process step is currently dirty; the system is being upgraded to improve cleanliness. An alternative hydrogen passivation procedure needs development for large area to achieve even lower leakage for small pixels.

f. Black Matrix

Process is under control for etching the amorphous silicon. It is under development for the underlying nitride.

5. Device Characteristics for the Sarnoff Polysilicon Process

Various electrical parameters are measured on each lot that is produced in our large area facility. The most important of these are threshold voltage, leakage (off) current and drive (on) current. Figure 12 shows the values of N-channel and P-channel threshold voltage as a function of time. As seen from the data, the threshold values are about $^{+}$8V(N) and $^{-}$12V(P).

The variation in N- and P-channel drive currents as a function of time is shown in Fig. 13. The minimum acceptable level for proper operation of the LCD arrays is 1 μA. As is seen from the data, most of the recent transistors have drive currents considerably above this level.

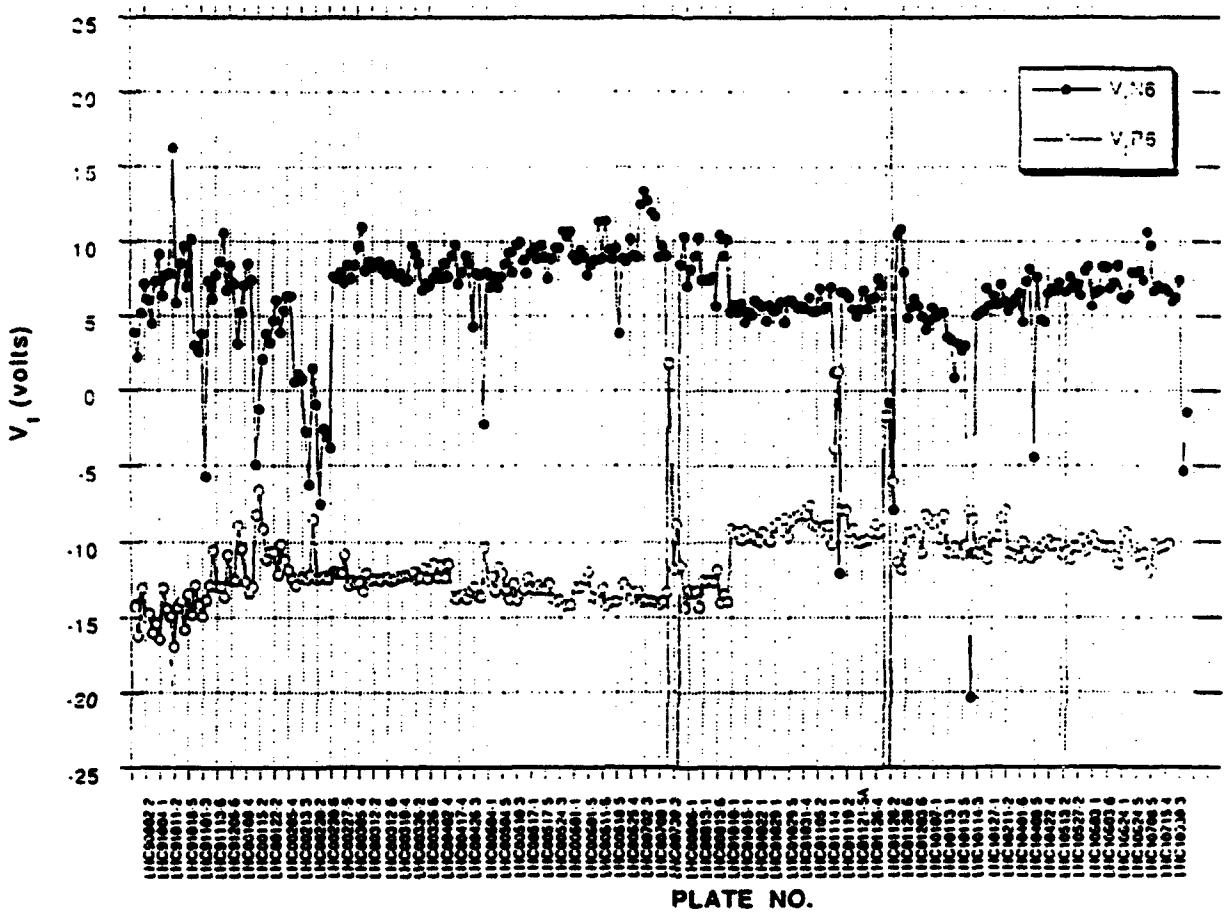
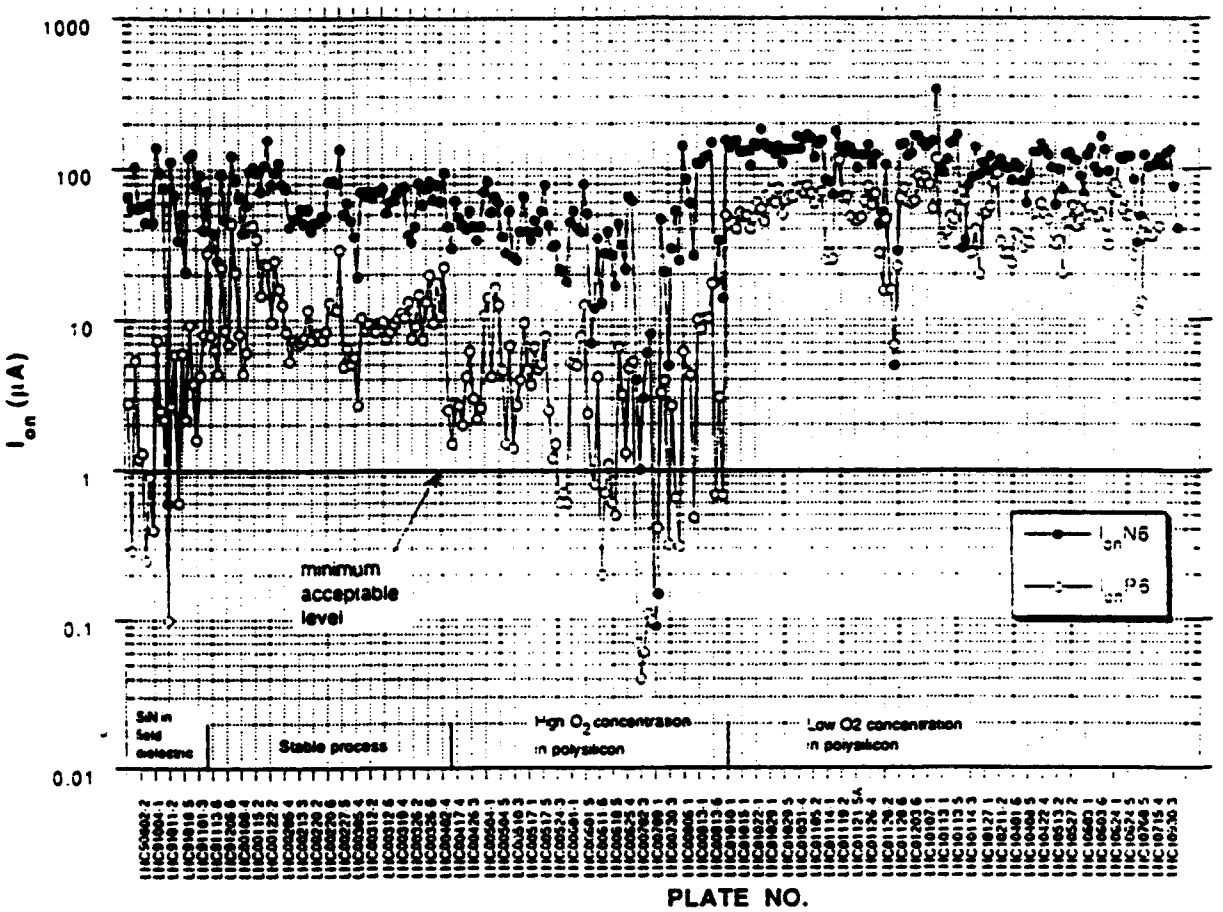


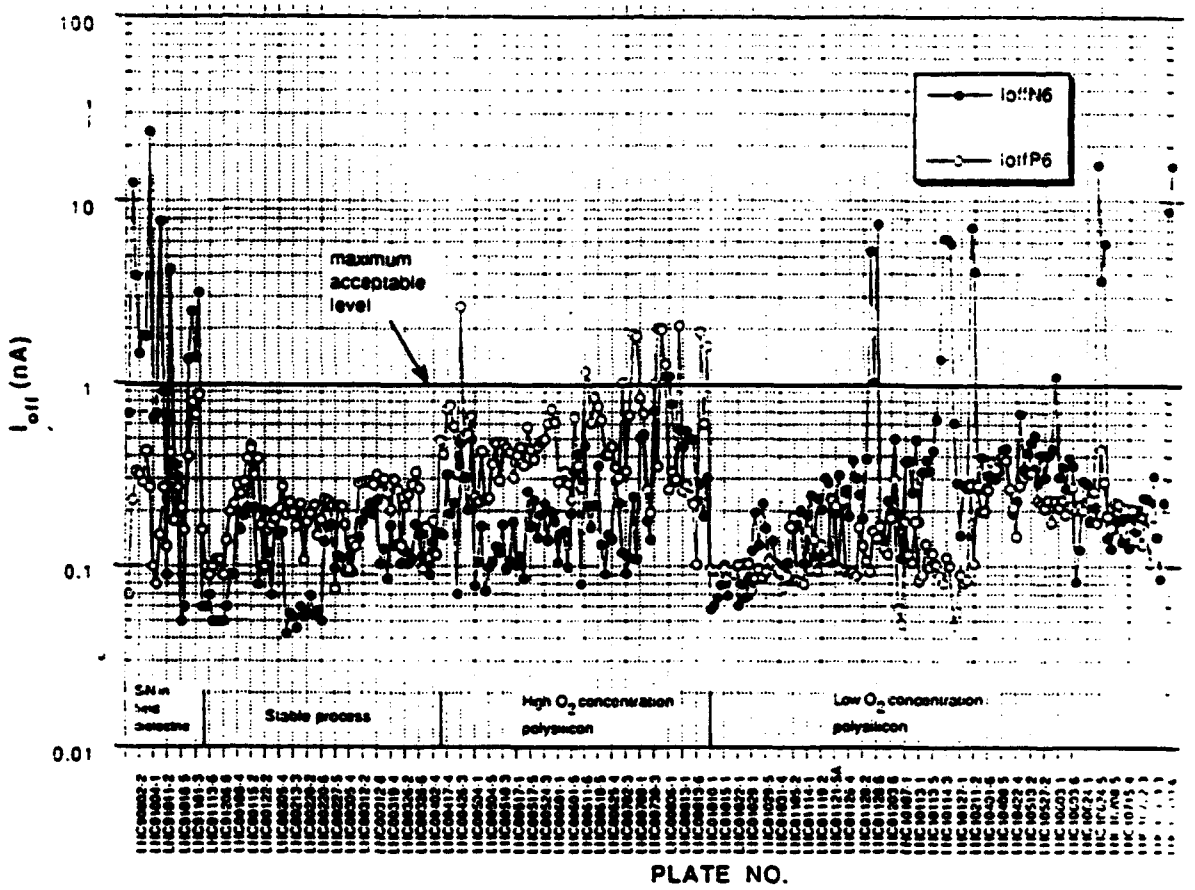
Figure 12. ***N- and P-Channel Transistor Threshold Voltages as a Function of Time.***



Channel lengths are 6.0 μm, and channel widths are 10 μm.

Figure 13. ***N- and P-Channel Transistor Drive Currents as a Function of Time.***

Figure 14 shows N- and P-channel transistor leakage currents as a function of time. The maximum allowable leakage level depends on the application. We have arbitrarily chosen 1 nA as the maximum value for which we will consider plates as a candidate for repair and assembly. As is seen in the figure, the leakage levels of recently fabricated devices are well below this limit except for occasional experimental lots.



Channel lengths are 6 μm, and channel widths are 10 μm.

Figure 14. ***N- and P-Channel Leakage Currents as a Function of Time.***

5. DISPLAY SYSTEM

5.1. GENERAL

The delivered display system is composed of three major units as shown in Fig. 15. The first unit is the Support Electronics System (SES) that houses all of the power supplies and electronic circuits for accepting the video input signals, processing them, and driving the Color Head Down Display (CHDD). The second unit is the LCD mounted in a metal bezel and attached to the front of the color sequential backlight. The third unit is the programmable video generator manufactured by Leader.

5.2. SUPPORT ELECTRONICS SYSTEM

The purpose of the SES is to accept analog RGB component video information from a video source, digitize it for storage and reformatting, and deliver it to the CHDD in the proper sequence for display in the color sequential mode. The block diagram for the final system is shown in Fig. 16.

Three possible video sources can be connected to the SES equipment rack for selection from a front panel control. All three require RGB and composite sync signals. The first is the low-resolution signal that conforms to the RS 170A sync standard. The second is from the supplied Programmable Video Generator that is set by the contractor for the best match to the best resolution and timing for the CHDD. The third, which is not called for in the contract, should allow connection to the Wright Laboratory simulator video sources.

The RS 170A video is a low-resolution source with many undesirable visual artifacts. There is no need to electronically enhance the signal to match the full capabilities of the head down display for this contract. The RS 170A standard, however, is a simple and convenient source of video to test the dynamic characteristics of the display. The most cost-effective scheme was to use the video as is without any enhancing video processing and to limit the amount of additional electronics in the SES to accomplish this.

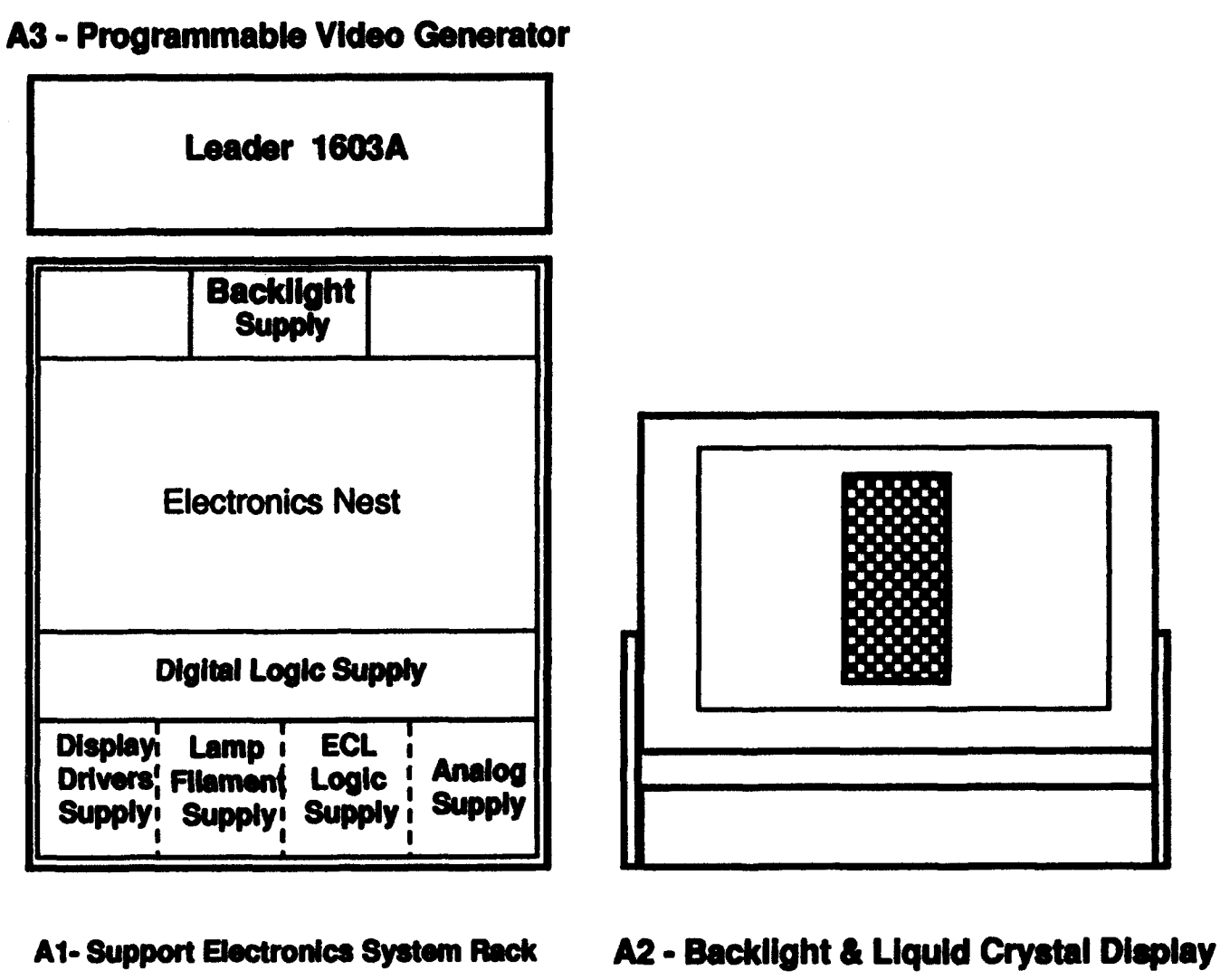


Figure 15. *Major Units for CHDD System.*

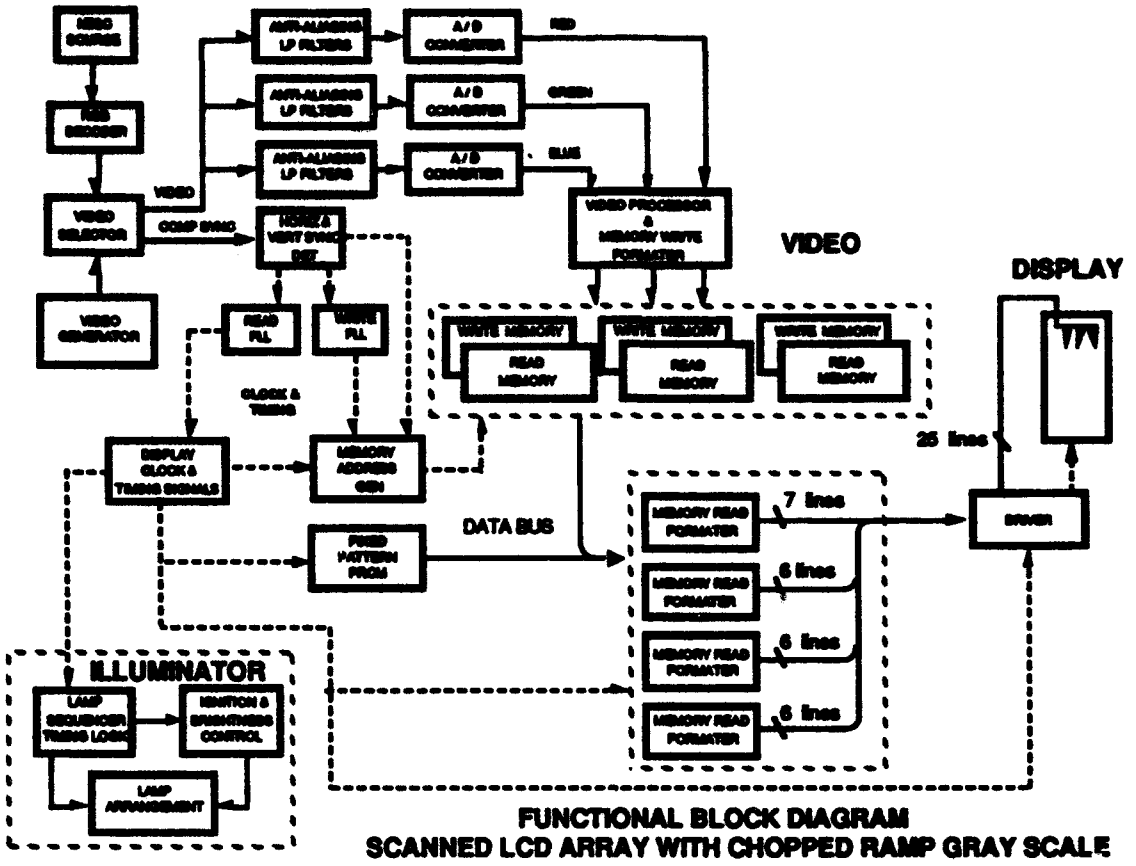


Figure 16. *SES General Block Diagram.*

The composite sync signal is separated into its horizontal and vertical components. A pair of Read and Write Phase Locked Loop (PLL) oscillators are locked to the horizontal signal. These circuits drive all the clock generation and timing signals required by the system. The Write PLL drives all the circuits up to and including the inputs to the Frame Buffer Memories and the Read PLL drives everything after these memories. The vertical signal is used as a system reset to initialize each cycle period.

The video selector connects the three analog video signals from the desired source to the anti aliasing low pass filters. These signals are then amplified according to the settings of the black level and picture level controls located on the CHDD and backlight assembly. The three signals are then digitized by three A/Ds at approximately a 40-MHz rate into three corresponding 6-bit words. The LSB of each word is discarded since the system requires only a 5-bit accuracy.

The original plan was to build a three-section tiled display that was 12 in horizontally by 8 in vertically. This was later down scoped to a single 4-x 8-in display. The front end of the SES electronics was not down scoped and still digitizes the incoming video for display on the 12 x 8

format. This means that each horizontal line is sampled approximately 1200 times, and all the samples are sent to the video write formatter. The first 400 and last 400 samples per horizontal line, are passed to an open connector and are lost. The center 400 samples/horizontal line are fed through to the six frame buffers. These samples are reformatted by stacking four consecutive 5-bit words into a single 20-bit word for the SES input data bus.

The buffer memory is composed of six separate frame buffers, two for each color. The two frame buffers for each color are then operated in a manner so that while one is being written into, the other is completely free to be read from. This ping-pong operation was selected for maximum independence between the Read and Write modes providing flexibility to accommodate a 90° image rotation if required. This memory structure also allowed a simple method of providing a video freeze frame mode of operation that is helpful in image analysis.

The output video information from the frame buffers are reformatted in the four parallel-to-serial reformatters for the high-speed clocking (8 MHz) to the CHDD. These reformatters intermix the data words and the five bits for each word for proper demultiplexing of the 4:1 demultiplexers in the on-glass circuitry of the display.

The read clock is used to generate all the timing, control, and clock signals for the display and the backlight controller. The data clocks, select clocks, gray-scale clocks, and data signals are level shifted by the driver circuit and fed to the display.

5.3. LIQUID CRYSTAL DISPLAY

1. Grayscale

The LCD was fabricated, tested, and repaired in the facilities at Sarnoff and then assembled under a subcontract by Standish Industries.

The display grayscale operation was evaluated on a test bed and showed a monotonic operation for each of the 32 codes for its 5-bit D/A design. This is shown in Fig. 17.

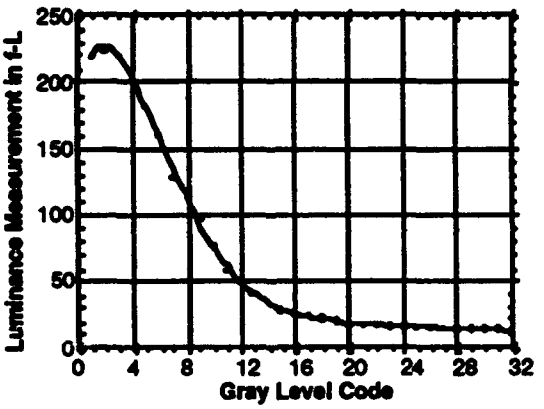
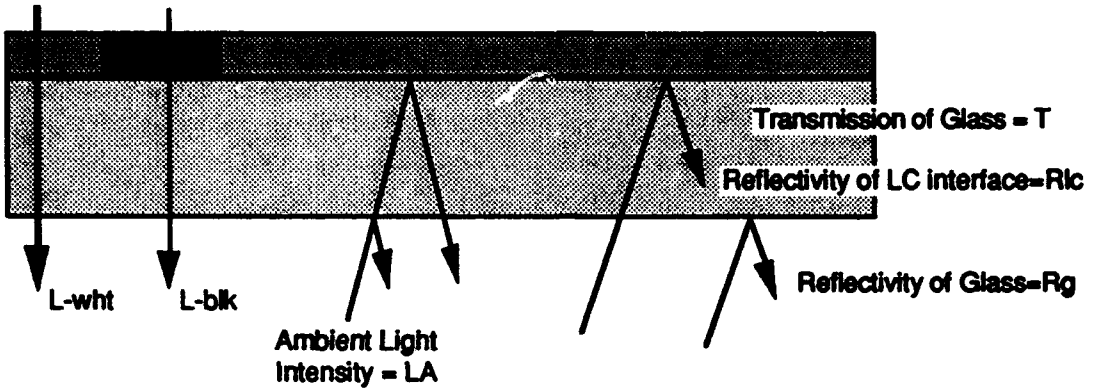


Figure 17. *Chopped Vamp D/A Operation.*

2. Contrast Ratio

The contrast ratio is defined as the light intensity that reaches the viewer in the liquid crystal "on" state or "white level" divided by that reaching the viewer in the "off" state or "black level." Figure 18 is a simplified diagram of the main components of the transmitted and reflected light of a display being viewed under some ambient light conditions. The contrast ratio is the sum of the "on" state light (L-wht) and the reflected ambient light components divided by the sum of the "off" state light (L-blk) and similar reflected ambient light components. The reflected ambient light components are a function of the reflected interface components and the transmission of the glass. The reflectivity component at the LC interface may be different for a white and black pixel in the display, but this difference negligible for this discussion.



$$\text{Contrast Ratio} = \frac{\text{L-wht} + \text{LA} \cdot f_{(Rg,Rlc1,T)}}{\text{L-blk} + \text{LA} \cdot f_{(Rg,Rlc2,T)}}$$

Figure 18. *Contrast Ratio Measurement.*

Table 7 lists the contrast ratio measurements under both a checkerboard pattern and full white and black fields. With the checkererboard pattern, the display has changing signals on the display vertical data lines.

We can infer from this table that the ambient light reflective function has a value of approximately 0.008. This would make the contrast ratio for a 10,000-fL ambient equal to 2.8:1 for both checker and full field patterns.

TABLE 7. Contrast Ratio

	Checker Pattern	Wht Field/Blk Field
Dark Ambient (3 fL) Contrast Ratio	179 f-L / 11 f-L 17:1	149 f-L / 3 f-L 51:1
High Ambient (375 fL) Contrast Ratio	179 f-L / 15 f-L 12:1	154 f-L / 6 f-L 24:1
Very High Ambient (3500 fL) Contrast Ratio	205 f-L / 45 f-L 5:1	176 f-L / 28 f-L 6:1

5.4. COLOR SEQUENTIAL BACKLIGHT

1. Operation

Figure 19 shows the major components of the CHDD assembly. Like other fluorescent backlight display assemblies, it consists of a light source along with its power source, an LCD, and a light distribution technique to evenly distribute the light to the display assembly. In this system, however, the light source is composed of 24 fluorescent lamps, grouped as 3 sets of 8 lamps, 1 set for each of the primary colors red, green, and blue.

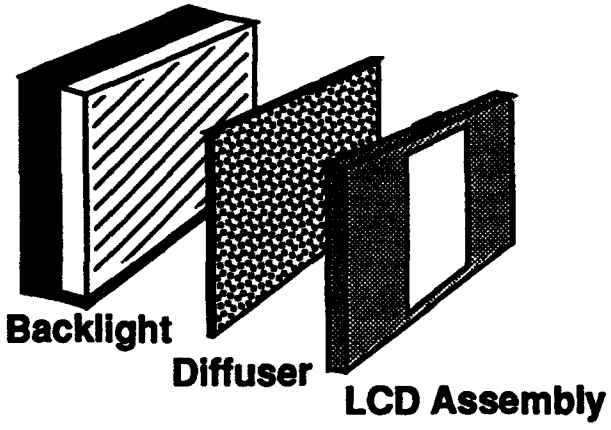


Figure 19. *Major Units for CHDD System.*

The power supply provides each lamp with a separate current control to balance its individual light output. Finally, there is an overall control to set the average brightness of the

display. Each lamp has a separate switch control in the power supply that is controlled by the logic sequencing of the video drive electronics to the LCD. In this manner, the exact turn-on point and length of on-time for each lamp is externally controlled in relation to the other display sequencing.

The types of fluorescent lamps used are reflector types purchased under a subcontract from GTE. These lamps have internal reflective coatings between the bulb wall and the phosphor coating. A narrow slit runs lengthwise along the bulb to create an exit port for the light. This exit port has a phosphor coating in the reflector bulb but is left clear for the aperture lamp. These lamps are slightly less efficient than normal fluorescent lamps due to their small diameters and high currents, but the narrow beam light output characteristics make them ideal for this application.

A simple diffuser was the original technique planned to be used to distribute the light evenly to the rear of the LCD assembly. It is recognized that some brightness and uniformity of the display is lost, but the cost of the optics for this step verses the qualitative results of the displayed pattern was of primary concern .

The operation of the field-sequential color system is illustrated in Fig. 20. For a typical horizontal interlaced 30 frames/sec video source, six color fields are created. There is one odd and one even field for each primary color called Ro, Go, Bo, Re, Ge, and Be, as shown. These signals are electronically stored in the display electronics, reformatted, and loaded into the display.

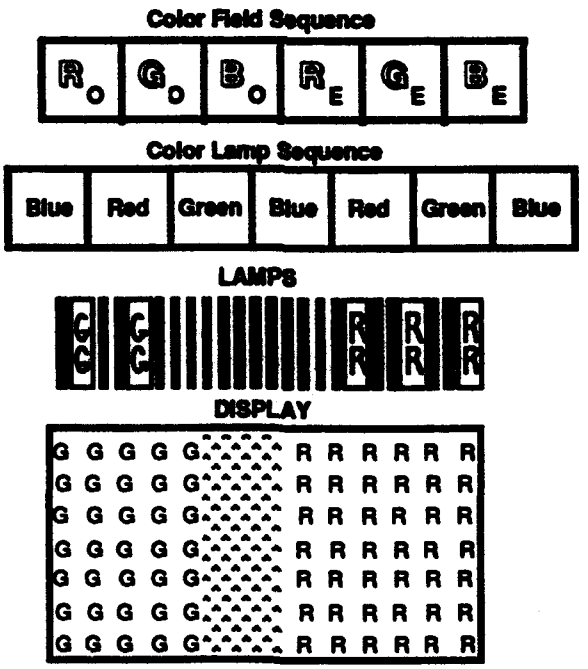


Figure 20. *Video and Backlight Sequencing.*

Each LCD cell is a capacitor and stores information as a charge in that cell. Although this charge will leak off eventually, at normal field cycle times, old information will remain valid until over written by new information similar to a dynamic memory. This means there will be a boundary moving down the display with previous color information on one side and new color information on the other side. Because of the slow response time of the liquid crystal material, this will not be a sharp line of demarcation, but a band of an indeterminate state.

The color lamps are sequenced in the same R-G-B order and are phased, so that the liquid crystal material has time to approach steady-state condition following each video change.

Liquid crystal displays require ac pixel voltages to prevent image retention. In this system, the phase of the data is reversed every other horizontal line. For a given horizontal line and any given color field, the fundamental repeat pattern for a still image will be at 15 Hz. This is illustrated in Fig. 21.

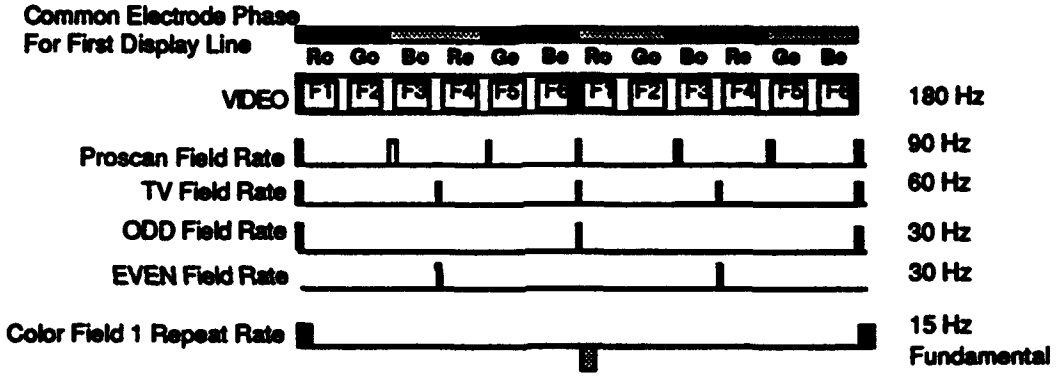


Figure 21. *Video and Backlight Sequencing.*

Any ambient light that passes through the display and diffuser, could be reflected out of the backlight housing along with the desired color light coming from selected fluorescent lamps. This will corrupt the correct color of the display. In the case of a white ambient light, this will desaturate the desired color. To minimize this, the backlight interior surfaces are painted a flat black. The phosphor coatings of the fluorescent lamps reflect white light. To minimize this, the lamps could be sleeved in a color filter that is matched to the spectral output color of the corresponding lamp.

2. Lamp Characteristics

A fluorescent lamp produces an energy transfer from electrons accelerated through an electric field to a low pressure mercury plasma. About 60 percent of the input energy is converted

to the emission of UV light at a wavelength of 2537 A. The inner surface of the lamp is coated with phosphors selected to transform the 2537-A light down to the desired color light. A given phosphor can only absorb and convert to useful visible light, electromagnetic radiation within a specific wavelength range at an efficiency of about 45 percent. In addition, there is a bulb and phosphors absorption loss of about 15 percent.[7] Couple these efficiencies with the average luminous efficiency for a white fluorescent light of about 57 percent and the resultant maximum luminous efficiency of 680 lumens/W for 5550-A light is reduced to about 88 lumens/W. The small diameter, short length aperture and reflector style lamps are less efficient than this and are rated at 60 lumens/W in a continuously operating mode.[8]

The process that produces the initial electrons is important to the lamp efficiency and life. There are two types of electron emission used in present commercial ac lamp operation, thermionic emission or hot cathode and cold cathode. The hot cathode has a life expectancy of 5000 to 15000 hours while the cold cathode has a life of 10,000 to 20,000 hours. The hot cathode has a "cathode fall" potential, which is part of the cathode loss factors, of 12-15 V while the value for the cold cathode is 120-150 V. Although the cold cathode lamps are known for their long life, ability to tolerate high peak currents, short duty cycles, and have a large dimming range,[9] they are not desirable in this application. This is because of a long unlit area at the ends of the tubes and the higher starting voltage required to strike the plasma.[10]

The color-sequential system requires a pulse-type mode of operation that also infers the need for a hot cathode because of the operating speeds needed. This continuous heater power will decrease the efficiency value. A heater element is required at each end of the lamp for bidirectional current flow to prevent mercury migration within the lamp. Some form of alternate end heating and operation is required to minimize this energy loss. These heaters consume 1 W each.

Dimming of fluorescent light sources can be accomplished either by controlling the current to the lamp or by controlling the duty cycle of the drive signal when the lamp is operating in a pulse mode.

Varying a lamp current from 1 to 100 mA should give a dimming range of just under 1000:1 as shown in Fig. 22. The data for this figure were taken from a yellow-green fluorescent lamp and show that the additional dimming range for a 4000:1 ratio can be obtained by controlling the duty cycle of the lamp.

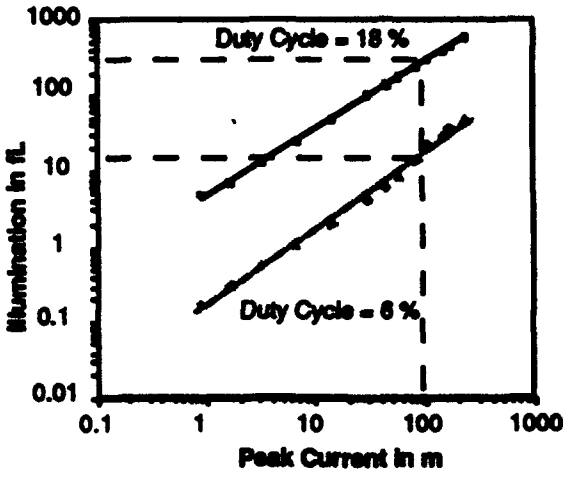


Figure 22. *Lamp Dimming Range.*

Because of the cost restraints, we used the lamp control units available from the lamp manufacturer. These ballast units were restricted to the 100-mA peak level of operation and had no means of current control. Measurements of the actual backlight brightness levels with the LCD, while operating in the pulse mode, are listed in Table 8.

TABLE 8. Backlight Luminance Measurements

Ambient fL	Color PS Max fL Duty cycle = 20%	Color PS Min fL Duty cycle = 2%	Ratio Max/Min	Monochrome Max fL Duty cycle = 40%	Monochrome Min fL Duty cycle = 6%	Ratio Max/Min	Max Continuous Duty cycle = 100%
1	151	5	31:1	235	16	15:1	623

Backlight plus display in white field

LCD Transmission = 15%

The color gamut of the backlight is shown in Fig. 23 on a CIE chromaticity diagram. The measured coordinates are listed in Table 9. This covers a larger area than is possible with the presently available color filters.

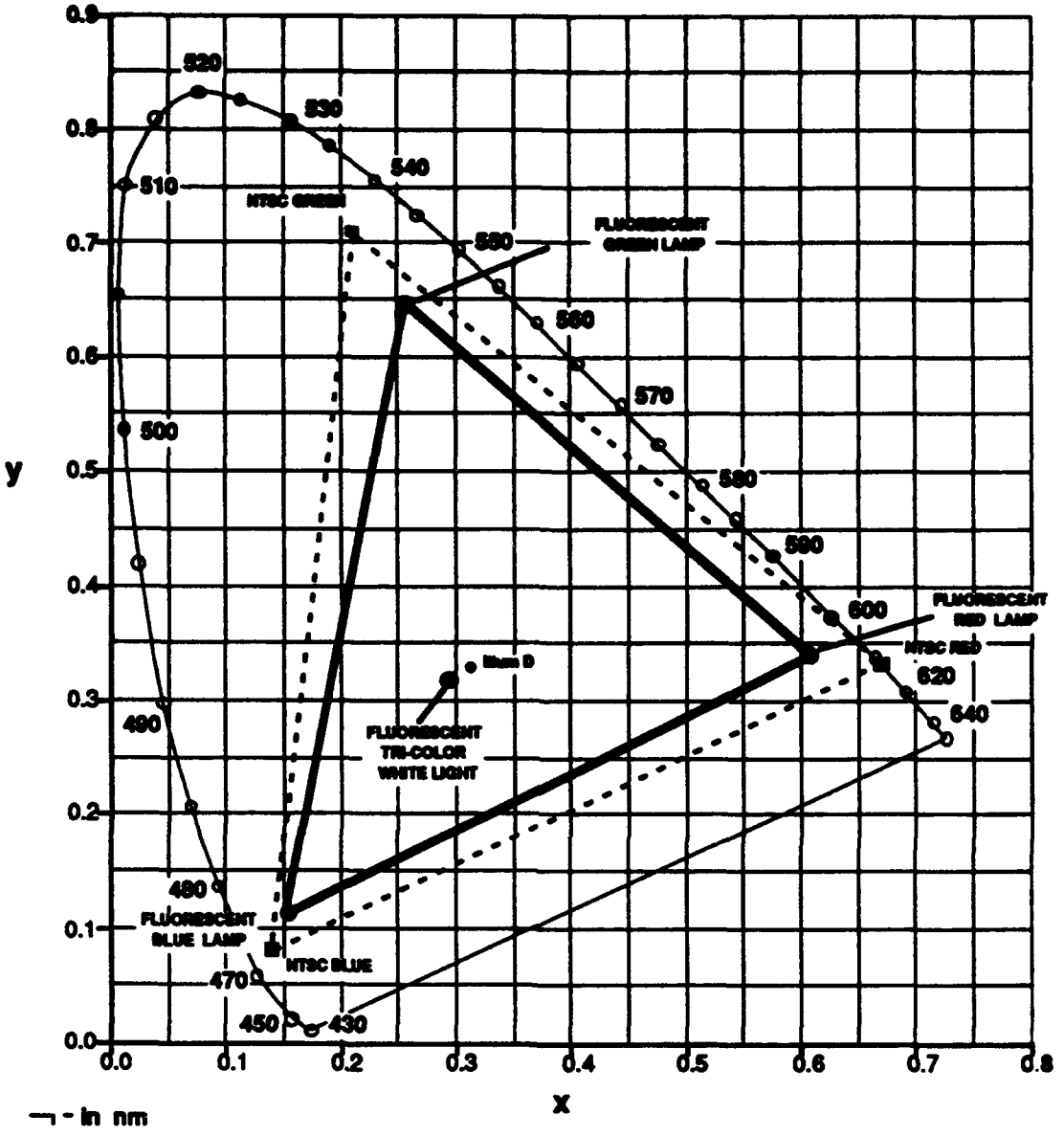


Figure 23. *CIE Chromaticity Diagram.*

TABLE 9. CIE Lamp Coordinates

Coordinate	Red	Green	Blue	R+G+B
x	0.6015	0.2579	0.1556	0.2903
y	0.3397	0.6475	0.1114	0.3171
u'	0.4096	0.1006	0.1546	0.1865
v'	0.5206	0.5683	0.2491	0.4585

3. Diffuser Characteristics

A common type of opalescent plastic diffuser was originally planned to be used in this backlight. This type of diffuser had a good lateral uniformity and generally gave a Lambertian distribution of intensity as a function of angle. Late in the program, samples of a special Rohm Haas[11] diffuser were received. Figure 24 shows the preliminary test results obtained from these samples.

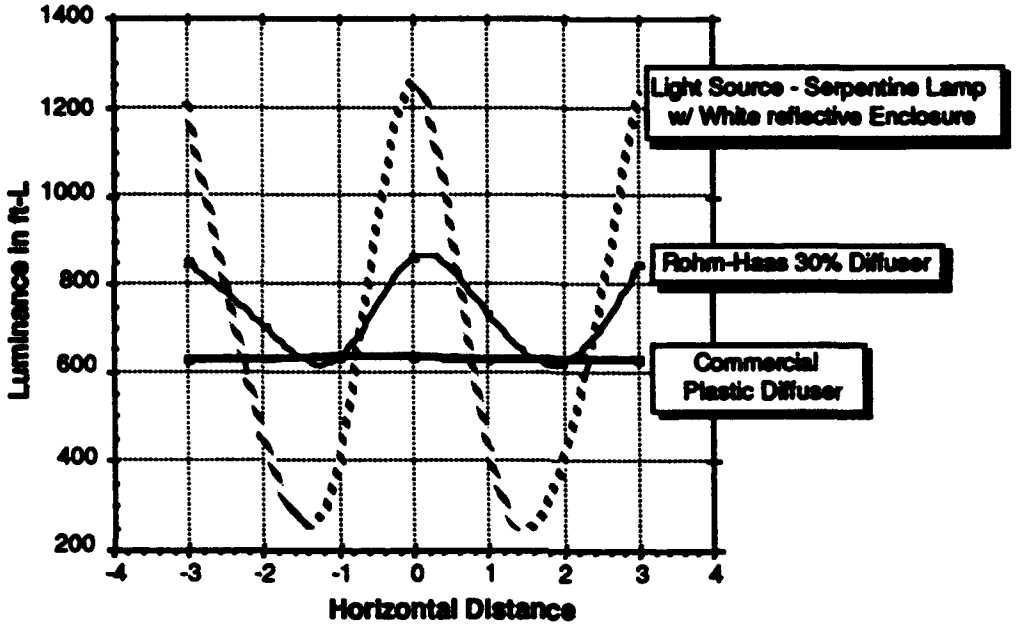


Figure 24. *Diffuser Plots.*

Compared to the average luminance output of the lamps along the horizontal axis, the Rohm-Hass has very little attenuation while the ordinary plastic diffuser had an attenuation of about 20 percent.

A more sophisticated holographic diffuser was also studied for this program. The advantage of this diffuser is that it can scatter collimated light into a beam having a well defined angular distribution with negligible absorption. Its disadvantages are its high cost and performance that is strongly dependent on wavelength.

We had a free sample of a Physical Optics diffuser that provided diffusion in only one axis. Figure 25 shows a comparison between the sample of this type of diffuser that we had and the Rohm-Haas diffuser. The Physical Optics diffuser showed no significant advantage over the Rohm-Hass diffuser especially since the costs of the Rohm-Hass diffuser is on the order of the ordinary plastic diffuser.

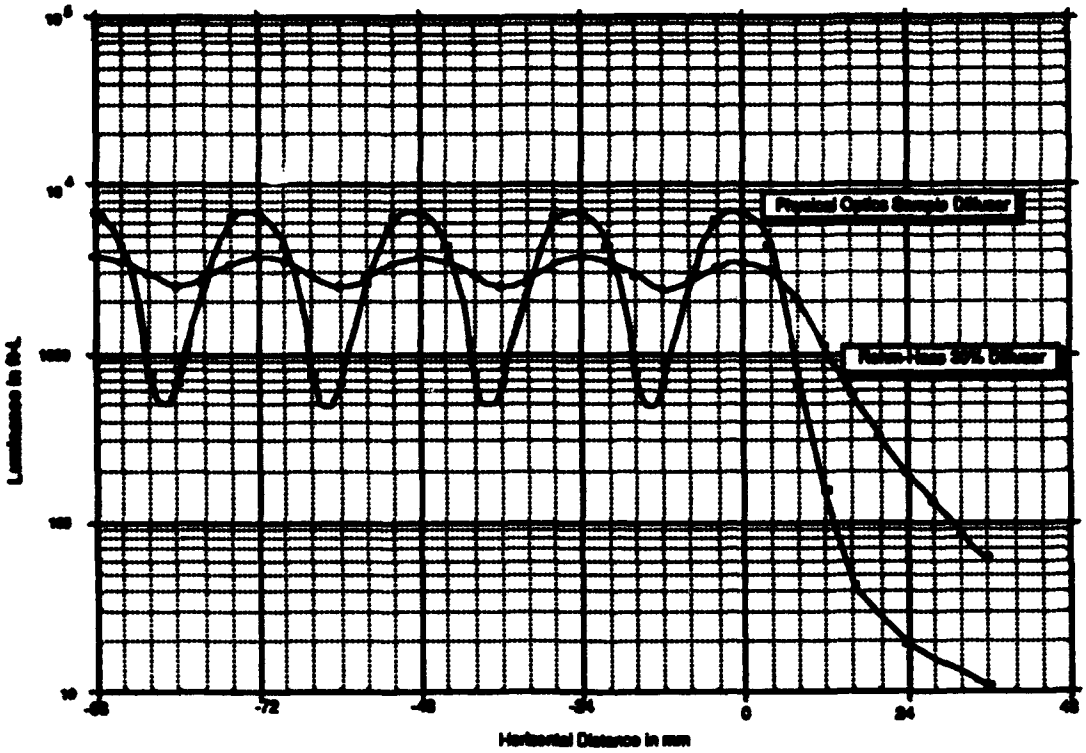


Figure 25. *Diffuser Plots.*

The final measured uniformity of the backlight in shown in Fig. 26.

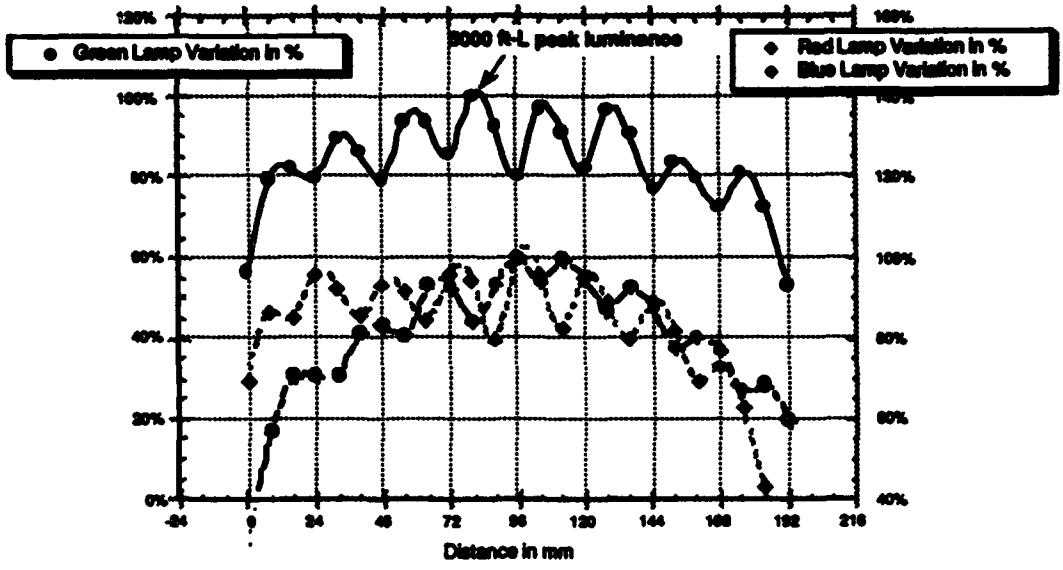


Figure 26. *Backlight Uniformity.*

4. Display Brightness

Figure 27 is a schedule of the light levels and losses through the color sequential display system. The aperture or reflector lamps have a back to front ratio of about 8:1. This reflective property of the lamps will concentrate about 60 percent of the light flux to the direction of the display.

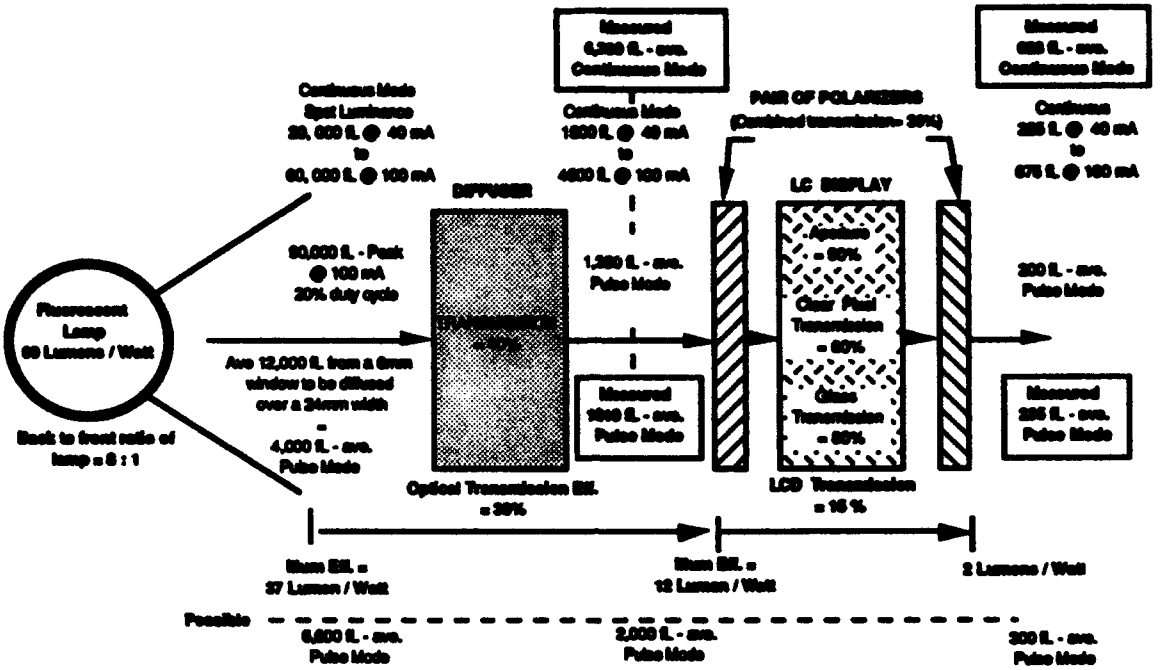


Figure 27. *Light Level Schedule.*

Presently, the reflector and diffuser losses give an optical efficiency of only about 30 percent. An optimization program to minimize the diffuser losses and to improve the reflector could double this efficiency to about 60 percent. Late in the program, a large free sample of the Rohm-Haas diffuser was received that we were able to mount into the bezel of the backlight.

The present LCD assemblies have transmission efficiencies of about 2 percent due to the color filter, polarizers, glass, and on-glass circuits. The more efficient Wright-Patterson pixel transmits about 3 percent through a 90 percent aperture pixel layout and reduced pixel electrode transmission losses. By eliminating the color filter, this efficiency will increase by an additional factor of 5. This should give a transmission efficiency of about 15 percent. When the display is optimized through reduced light valve losses, this efficiency could be increased even further. This would lead to an optimized transmission factor of at least 20 percent.

Based on this analysis, a minimum brightness level of about 200 fL was expected from this display system. A continuous mode of operation is also possible where all the lamps are turned on

to produce a bright white light. The luminescence levels are listed in the figure and show a maximum practical brightness level of 675 fL.

Actual measurements are also shown in Fig. 27 and show a lower luminance than expected for the pulse mode operation due to a smaller duty cycle, but a larger luminance level in the continuous mode of operation.

5. Color Sequential Timing

A three-lamp color-sequential experimental unit was assembled early in the program in order to study this concept. This multilamp illuminator, used 10-mm blue and green off-the-shelf commercially available fluorescent lamps and a red neon lamp. A 2-x 2-in LCD was assembled without a color filter. Figure 28 shows the timing relationships between the three component video signals, the firing points and time for each lamp, and the detected light from each lamp. This timing sequence produced the best full-field color bar pattern across a narrow band in the center of the display. This pattern included areas of white, yellow, cyan, and magenta demonstrating the proper temporal mixing of the color lights by the eye.

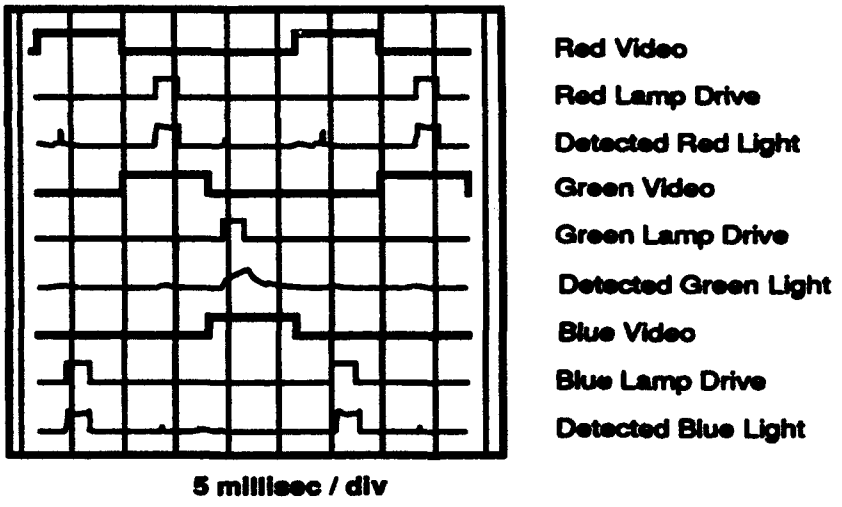
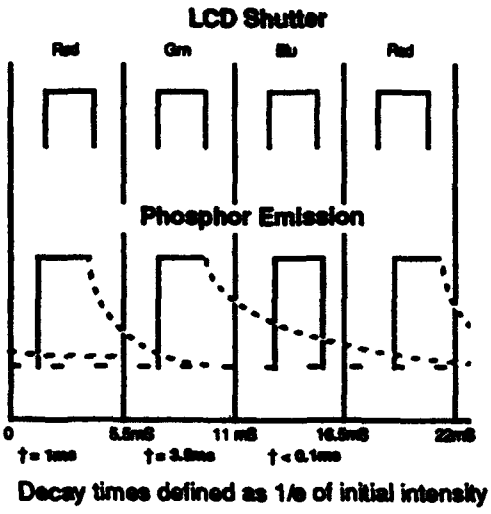


Figure 28. *Color Sequential Experiment.*

The final color-sequential backlight showed this same temporal delay between the loading of a particular color video information and the firing of the corresponding color lamps. This delay is due to the time constant of the liquid crystal material to react to the changing electric field. This delay in the firing of the appropriate lamps relative to the color information is not a problem since the system can be set up to operate with these fixed delays.

Sequencing through three successive different color video fields results in a low contrast image. When an LCD is sequenced through a series of identical video fields, the liquid crystal alignment can build to a final correct steady state and overcome the time constant delay. Distortion to the liquid crystal cell voltage due to the changing dielectric constant of the liquid crystal material as its alignment changes is also overcome with the repeating field information. The sequencing different color fields does not allow for this integration to a correct contrast level, and incorrect color light will leak through the display and cause a desaturation of the desired color.

The primary cause of color distortion in the color-sequential system, is due to the phosphor decay in the fluorescent lamps. This is illustrated in Fig. 29. This is an idealized situation where it is assumed that the liquid crystal light shutter is perfect, and the color information is aligned with the corresponding color lamp.



Amount of	Red	Green	Blue
In			
Red	1.000	0.088	0.000
Green	0.088	1.000	0.000
Blue	0.000	0.389	1.000
Total	1.088	1.397	1.000

Contaminated Colors

Amount of	Red	Green	Blue	
In				
Red	0.975	0.049	0.000	Reduced Red - 2.5%
Green	0.035	0.716	0.000	Reduced Green - 28%
Blue	0.000	0.235	1.000	
Total	1.000	1.000	1.000	Normalized for White

Figure 29. *Color-Sequential Phosphor Emission.*

When the fluorescent lamps are extinguished, the phosphor coating in the lamps will continue to phosphoresce. In the case of the blue lamps, this continued emission is in the microseconds and is negligible. The red lamps have a time constant around 1 ms, and the green lamps have a time constant of about 3.5 ms. This continued emission runs into the shuttered time for the other colors and contaminates them. This contamination is listed in the top table of Fig. 29 and shows that red will have some green impurity, green would have some red impurity, and blue would have a large amount of green corruption.

If the three sets of color lamps where adjusted and normalized for the best white, the color display would have the reds reduced by 2.5 percent and the greens by 28 percent. This would give the display the best black and white images but the color images would tend to look bluish.

6. SILICON TRANSFER PROGRAM SUMMARY

Functional single-crystal silicon 192 x 192 transmissive AMLCDs have been demonstrated. The 2.5-x 2.5-in display with integrated scan and drive functions was fabricated in a thin-film x-Si silicon-on-insulator (SOI) wafer using standard IC processing and subsequently transferred to glass. Comparison of device characteristics pre- and posttransfer shows that no degradation of device performance or introduction of defects is associated with this process. Measured device characteristics such as leakage current, transconductance, and speed are as expected for single-crystal silicon. Twisted nematic AMLCDs were assembled with this circuit using conventional techniques. This work focused on the use of x-Si because of the advantages discussed. However, the same technique could be used to fabricate displays using amorphous or poly-Si. Thin films of x-Si formed by other techniques, such as oxygen implantation (SIMOX) or wafer bonding, could also be used for AMLCD fabrication. The 192 x 192 AMLCDs fabricated with transfer silicon show excellent contrast ratio and picture quality. The speed, low leakage current, and high drive capability of single-crystal silicon devices should allow the fabrication of displays with integrated system-level peripheral circuitry, high pixel density, and improved contrast and optical aperture ratios.

6.1. INTRODUCTION

The conventional approach to AMLCDs relies on the fabrication of circuitry in thin layers of amorphous or polycrystalline silicon deposited on glass or quartz substrates. These substrates provide the optical transparency necessary for transmissive displays but the quality of the deposited silicon films limits circuit performance. The speed, low-leakage current, and high-drive capability of single-crystal silicon (x-Si) devices should allow the fabrication of high density displays with improved contrast and optical aperture ratios and integrated system-level peripheral circuitry. However, no technique has yet been developed to attain single-crystal quality silicon directly deposited in thin-film form on glass or quartz substrates.

Under this program, an approach for the fabrication of transmissive AMLCDs that allows circuitry to first be fabricated in thin-film x-Si, using standard IC processing, and subsequently placed on glass has been demonstrated. A functional monochrome 192 x 192 AMLCD with integrated drive and scan circuitry has been fabricated using this technique. While a transfer technique has been used to prepare a poly-Si display on glass,[12] this work demonstrates the first transmissive AMLCD formed from x-Si.

6.2. THIN-FILM x-Si MATERIALS

The starting material for circuit processing was thin-film x-Si prepared by the Isolated Silicon Epitaxy (ISE™) process.[13] In this process a thin film of x-Si is formed on an oxidized Si wafer (silicon-on-insulator material). As illustrated in Fig. 30, an oxide layer is formed on the surface of a standard single-crystal silicon wafer except for a small area near the edge of the wafer. The wafer is then coated with vapor deposited poly-Si and encapsulated with an oxide cap layer. The wafer is then uniformly heated to a bias temperature and scanned with a hot filament to directionally recrystallize the poly-Si layer using the original Si wafer as a seed to form a thin x-Si film on the buried oxide. The x-Si layer formed in this fashion has electronic properties comparable to a silicon wafer used for standard IC fabrication.[14]

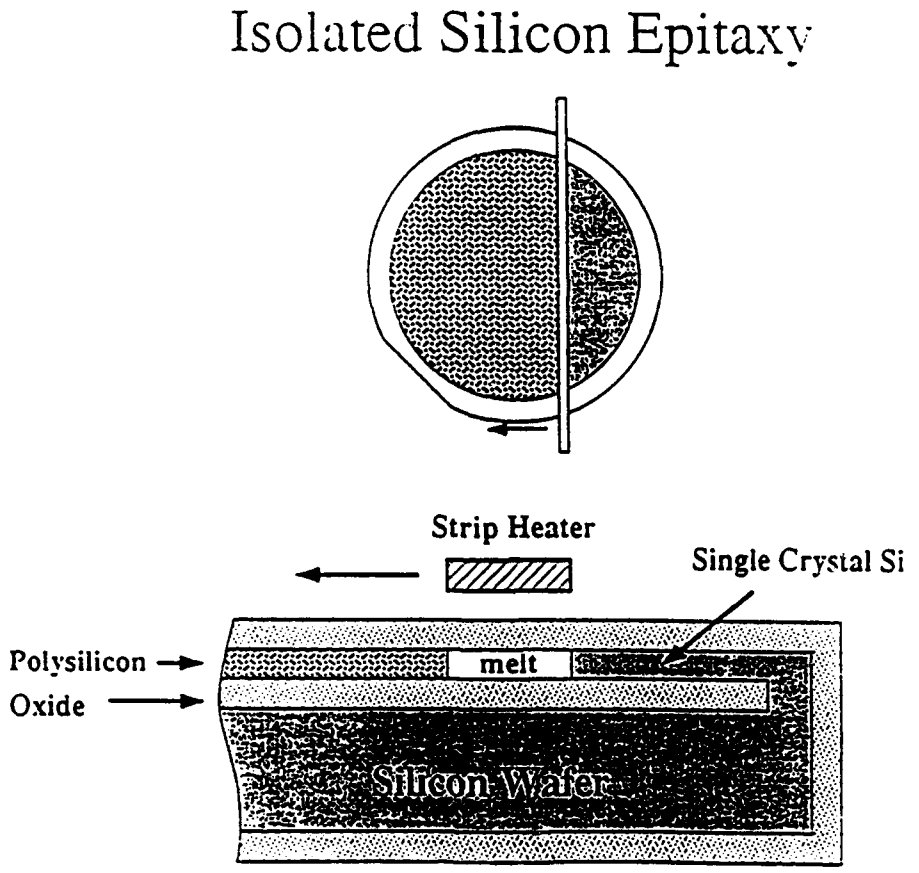


Figure 30. *Silicon-on-Insulator Materials Fabrication Process.*

After removal of the cap layer, circuitry can be formed in the thin x-Si layer using standard integrated circuit (IC) processes and equipment. The properties of the buried oxide layer can be used to facilitate removal of the x-Si layer, containing the integrated circuit, from the original Si water substrate.

6.3. DISPLAY FABRICATION

The display circuit used for this demonstration contained a 192 x 192 pixel active matrix with integrated drive and scan functions. This circuit design and layout had been developed for a polycrystalline silicon display.[15] The circuit processing sequence is illustrated in Fig. 31. The thin-film x-Si layer of the 4-in-diameter starting wafer was 0.3 μm thick on a 1-μm-thick buried oxide layer. The x-Si film was patterned using a dry etch technique to form Si islands that were thermally oxidized to form a 70-nm-thick gate oxide. Boron and phosphorus were implanted into the Si islands for threshold voltage control of the n- and p-channel MOS transistors. A layer of LPCVD polysilicon was then deposited at 560°C to a thickness of 0.5 μm and patterned to form the transistor gates. Phosphorous and boron implants were used to dope the source/drain regions and an APCVD Boron-Phosphorus-Silicon-Glass (BPSG) was deposited over the surface to form the interlayer dielectric. The wafers were then heated to 850°C for 20 minutes to flow the BPSG and activate the implants, contact vias were opened in the glass and reflowed, and aluminum metal was deposited and defined to form the interconnect pattern. A silicon nitride layer was deposited over the surface of the wafers prior to 450°C contact sintering. After array processing the wafers, some of the earlier wafers were neutron irradiated in order to minimize effects associated with the high carrier lifetime in the x-Si film. After a circuit redesign to add substrate ties, the neutron irradiation was eliminated from the process.

A unique feature of this display is that the pixel electrodes are formed from implanted x-Si, not poly-Si or ITO, resulting in a simplified process scheme. The x-Si layer has approximately four times the optical transparency of poly-Si films of equivalent thickness.[16]

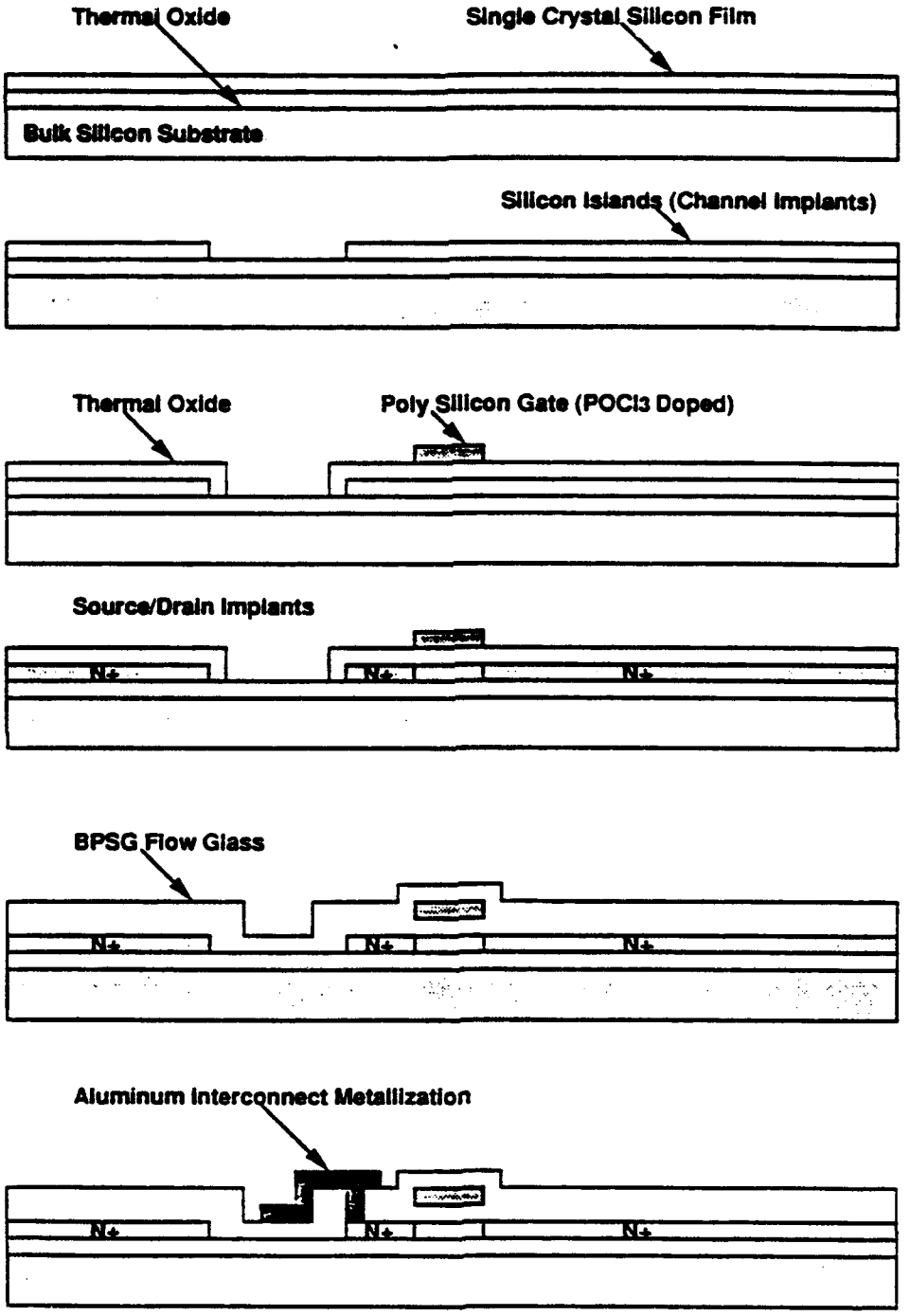


Figure 31. *Transistor Array Fabrication Sequence.*

After circuit processing, the 2.5- x 2.5-in integrated active matrix display circuit was removed from the silicon substrate and permanently bonded to glass using a thin layer of adhesive as shown schematically in Fig. 32. Both Corning 7059 and Hoya NA-40 glass were used. As a consequence of the transfer process, the original top surface of the circuit is placed adjacent to the glass and the back side of the circuit is exposed. Photolithographic processing is used post-transfer to expose the input contacts. The x-Si circuit is then put through a final test and laser repair procedure, normally done to the equivalent poly-Si circuits. These tests showed that the transfer process did not significantly increase the number of defects.

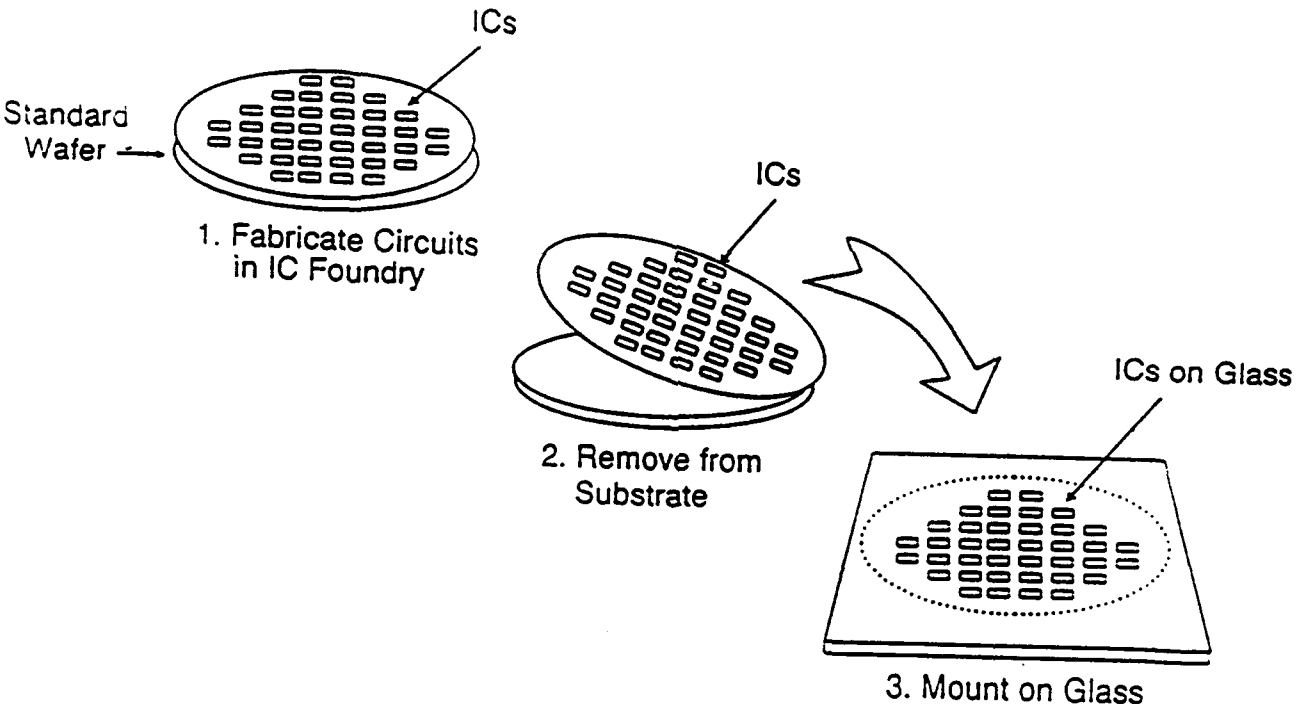


Figure 32. *Silicon Display Transfer Process.*

Processing of the glass-mounted x-Si active matrix circuit to make a twisted nematic LCD was accomplished through standard techniques. A preimidized polyimide was used as the liquid crystal alignment layer. This layer was rubbed in the conventional manner, resulting in about a 2° bias tilt. Spherical spacers were used to maintain a nominal 6-μm cell gap, and heat curing epoxy was used to achieve the perimeter seal. The cell was filled with liquid crystal by vacuum filling. Polarizers were then applied to make a normally bright, drive-to-dark display.

A schematic cross-section of the assembled display is shown in Fig. 33. No significant changes were required to assemble the transmissive x-Si display. Cell gap uniformity, seal integrity, and alignment stability compared favorably with standard active matrix cells.

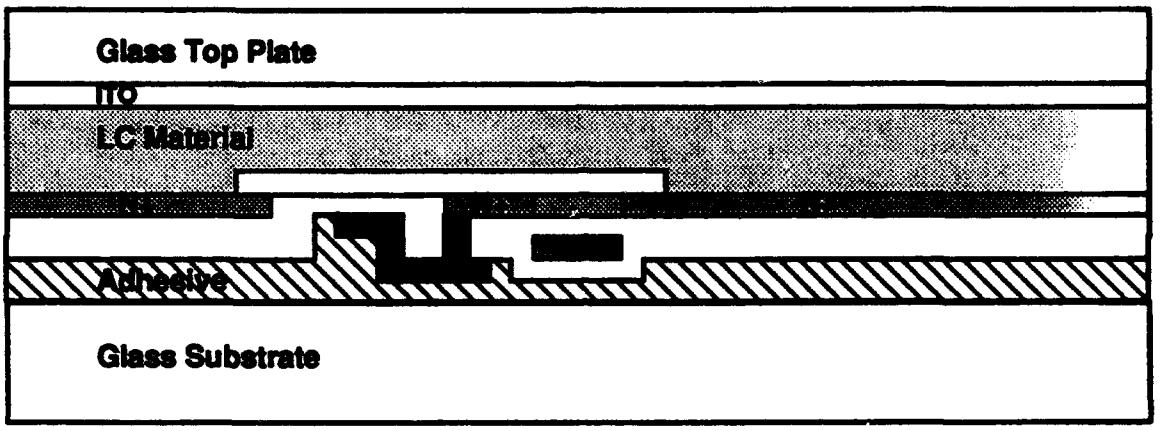


Figure 33. *Cross-Section of Transferred and Assembled AMLCD.*

6.4. x-Si-ON-GLASS DEVICE CHARACTERISTICS

The x-Si array fabrication and circuit transfer processes were evaluated based on the electrical characteristics of n- and p- channel transistors. Figure 34 shows typical n-channel subthreshold characteristics after x-Si layer transfer to glass. The characteristics before and after transfer were essentially the same. This is a single gate device having a gate length of 6 μm and gate width of 10 μm. The minimum leakage current is 0.06 pA/μm. The extrapolated threshold voltage for the n-channel device is 2.0 V, and the low field mobility is 467 cm^2/V-s. The p-channel device characteristics were similar to those of the n-channel device. The threshold voltage and low field mobility are, respectively, -1.5 V and 195 cm^2/V-s. Using the same size devices, inverter stage delays have been measured yielding a stage delay of 7.5 ns at V_{dd} = 5.0 Vm 2.0 ns at V_{dd} = 10 V, and 1.6 ns at V_{dd} = 15 V. The delays were essentially the same before and after transfer to glass. For comparison, typical parameters for low temperature polysilicon devices are $\mu_n = \mu_p = 20$ cm^2/V-s, VTn = VTp = VTp = +5 V, and r = 50=1-- n s at V_{dd} = 15 V.

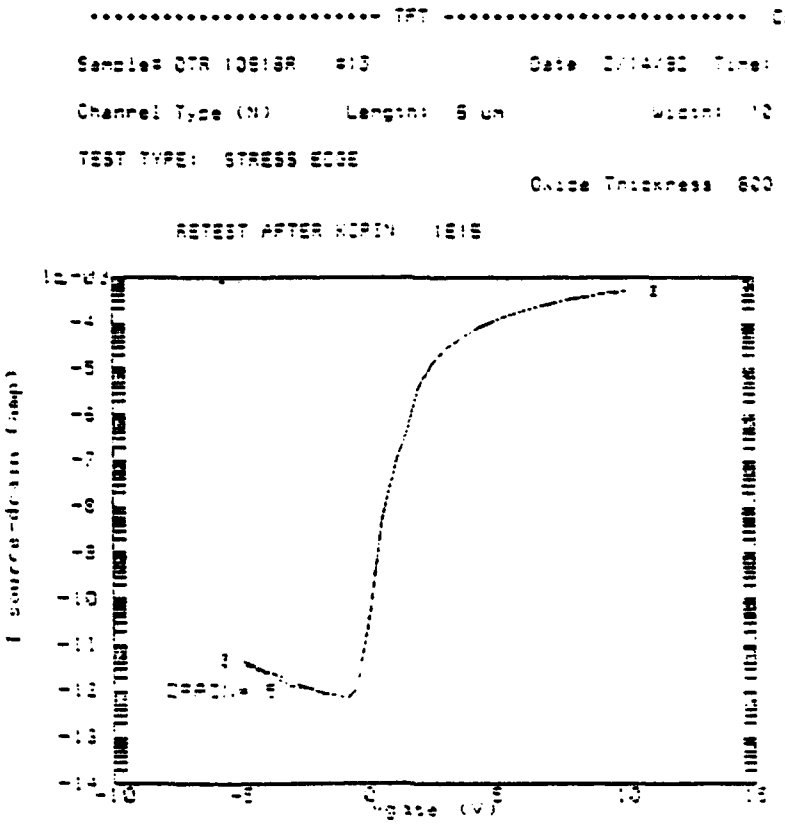


Figure 34. *N-Channel Transistor Subthreshold Characteristics.*

A problem with using x-Si devices for displays is the necessity for the devices to operate at voltages above 10 V. Unfortunately, x-Si SOI devices usually have a floating substrate region under the transistor channel and this region acts as a floating base of a bipolar transistor. The breakdown voltage of a floating base bipolar transistor is approximately 6-7 V, which causes problems for device operation in LCDs. Since we were anxious to prove out the transfer process for fabricating LCDs it was decided to use neutron irradiation for the couple of lots. Irradiation of silicon with neutrons is known to beta of bipolar transistors and, therefore, increase the breakdown of the SOI floating substrate MOS transistors. Figure 35 shows the breakdown voltage of n-channel MOS/SOI transistors as a function of neutron irradiation dose. As seen from the figure, the voltage was increased from an initial of about to 6-7 V to about 13 V for a gate length of 10 μm, which is the length used in the 192 design. There was also an increase in leakage current after irradiation, but we were able to reduce it by doing a postirradiation anneal.

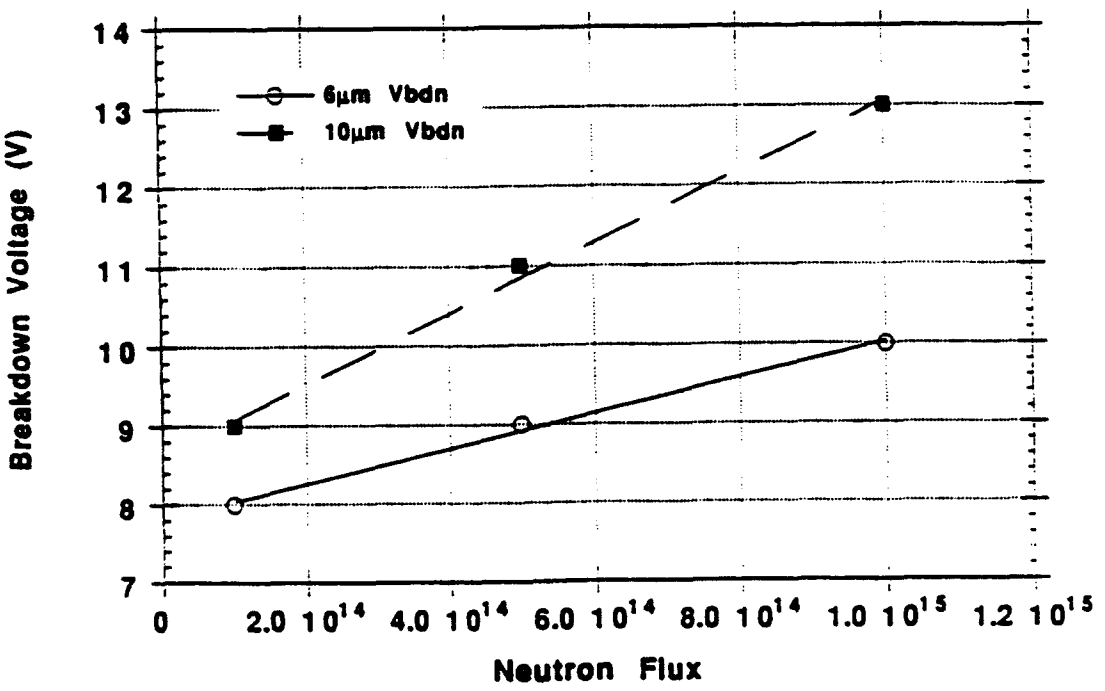


Figure 35. *Effect of Neutron Irradiation on Device Breakdown Voltage.*

In the redesign of the 192 array, substrate ties and multiple gate structures were added to the design. Measured data indicate that the breakdown voltage can be increased to about 12 V for 6-µm gate length devices. With multiple gates the breakdown can be increased by about 6 V for each gate added. A dual gate device, for instance, breaks down at about 12 V while a triple gate device breaks down at about 18 V. In order to achieve operating voltages above 12 V, therefore, it is necessary to use multiple gate structures. Additional techniques such as lightly doped drains can also be used to increase the breakdown voltage but they require process development. In summary, the redesigned 192 array was able to operate at approximately 12-13 V, which was sufficient to achieve displays with contrast ratios > 50.

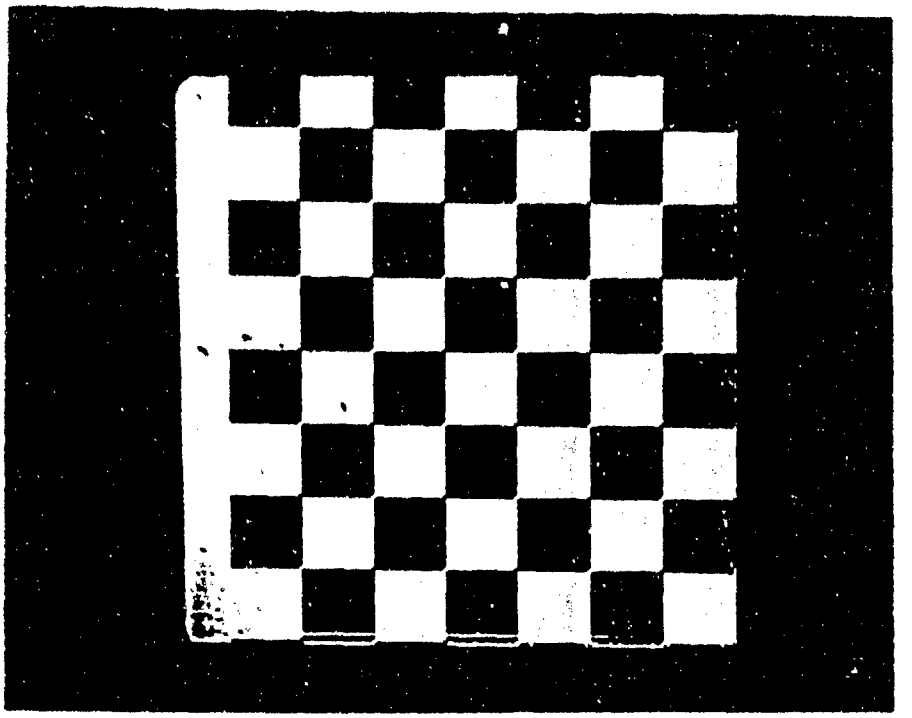
6.5. AMLCD CHARACTERIZATION

Figure 36 shows the operation of the world's first single-crystal silicon transmissive AMLCD. A checkerboard pattern is shown in the upper photograph and an all black pattern in the lower. This first display has greater than 85 percent pixel functionality. One of eight shift

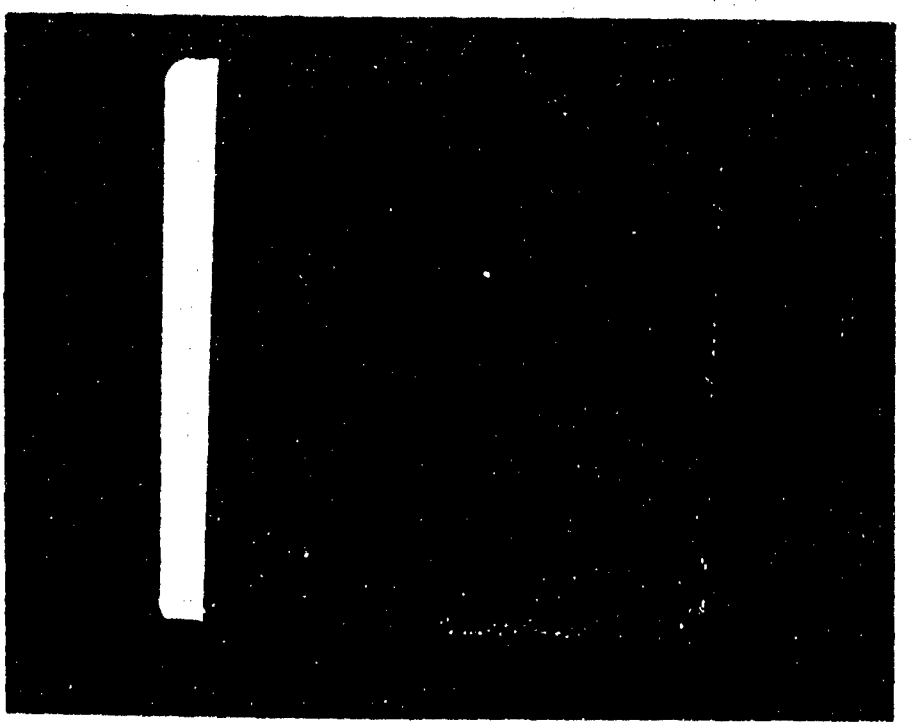
registers did not operate properly making the left-most 24 columns inoperable. Several discrete pixels, mostly near the right side of the display, were also inoperable. The pixel opens are believed to be due to over etching of the transistor contacts during array processing and not due to either the x-Si circuit transfer process or the LC assembly. The measured contrast ratio for this display, which does not contain a black matrix, is 4.7:1 using a pixel voltage of 4.8-V RMS. The calculated contrast ratio that would have resulted using a black matrix is 20:1. The display is normally operated at 180 frames/sec and a data clock rate of 1 MHz. The display also operates at the maximum data clock frequency, which the drive electronics can generate. This maximum frequency of 5.5 MHz produces a frame rate of 270 frames/sec. This display was assembled from the first lot of x-Si wafers and used neutron irradiation to achieve an operating voltage of 12 V.

Figure 37 shows a display from the third and final lot of processed x-Si SOI wafers. This display was fabricated using the modified mask set that contained body ties and multiple gate structures. No neutron irradiation was used to fabricate this display. As seen from the figure, there are no inoperable registers in either the data or select circuitry and very few pixel defects. This display was assembled using color filters and is available for demonstration at the Sarnoff.

Figure 38 shows micrographs of two different pixel arrays. The top micrograph of a standard poly-Si AMLCD pixel shows that disclinations (bright curved lines) form along the left side of the select lines. The disclinations are believed to be due to the interaction of the non planar surface and the electric field adjacent to the select lines. They occur along one side of the select line in the direction of the alignment layer rubbing. When very small pixels are used in an LCD, the bright disclinations are a significant contribution to a reduction in contrast ratio. The lower figure shows the same "all black" pattern on the single crystal transferred display. No disclinations are observed. The elimination of the disclinations is believed to be due to the planer surface over the select lines.



Checkerboard Pattern



All Black Pattern

Figure 36. *Photograph of World's First Silicon Transfer AMLCD.*

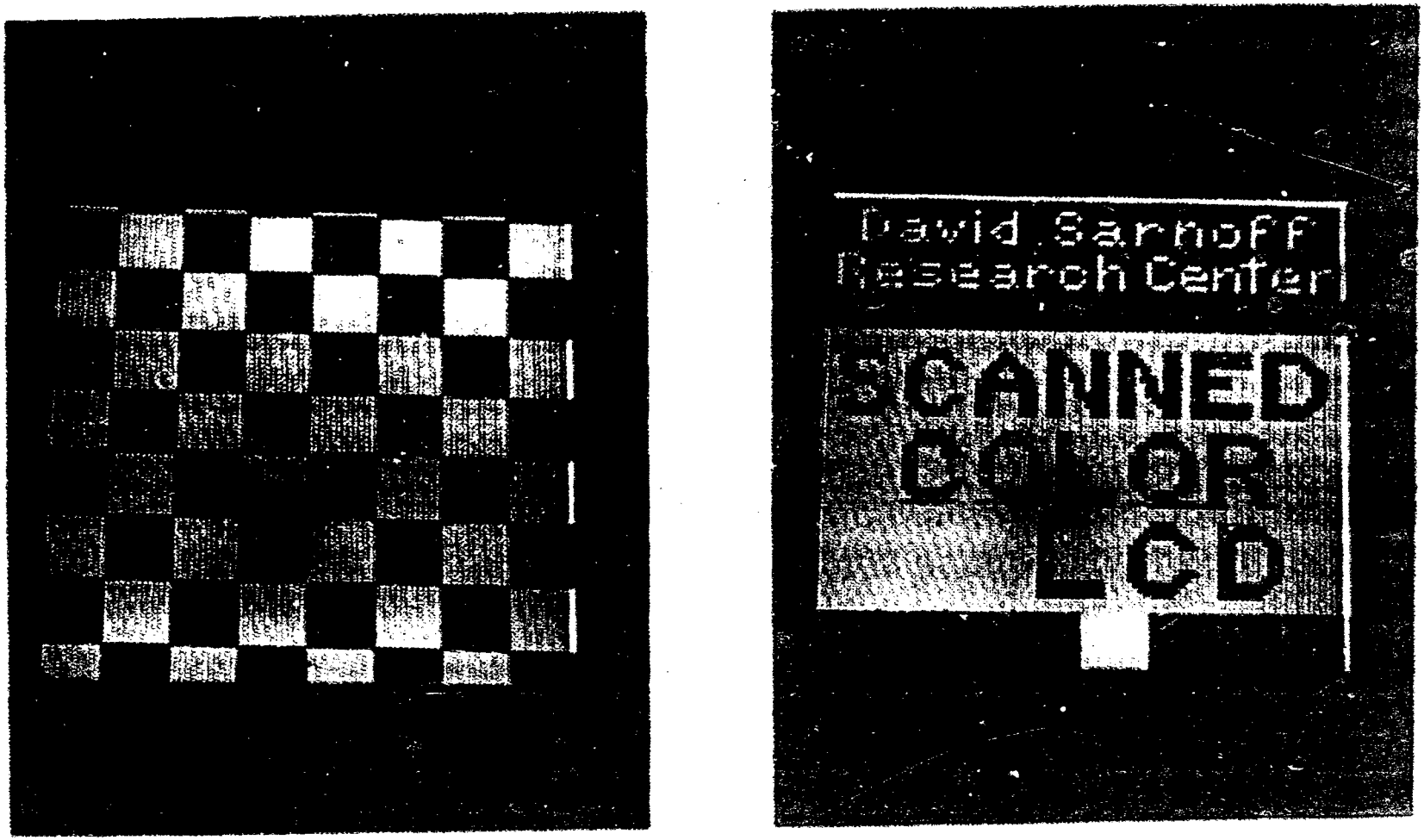
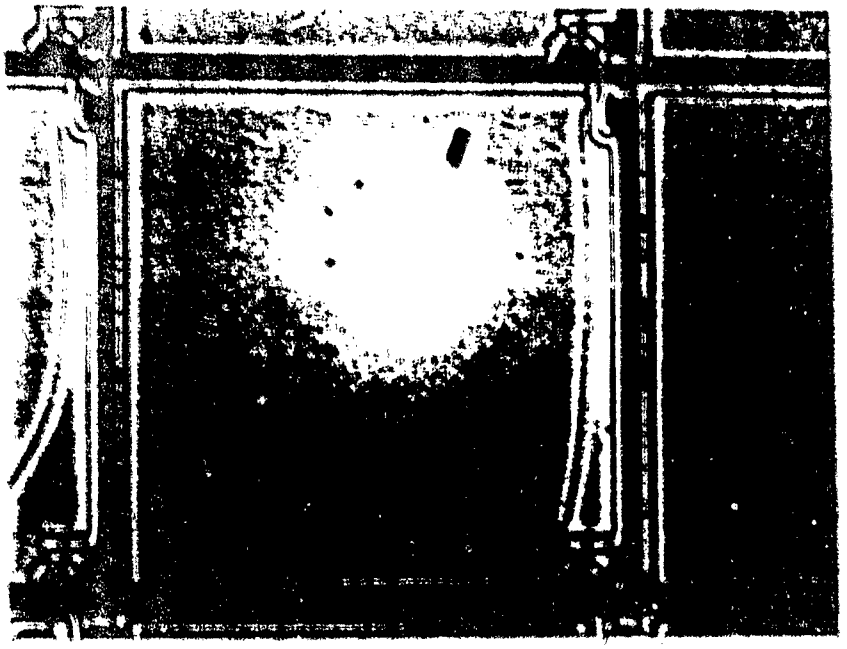
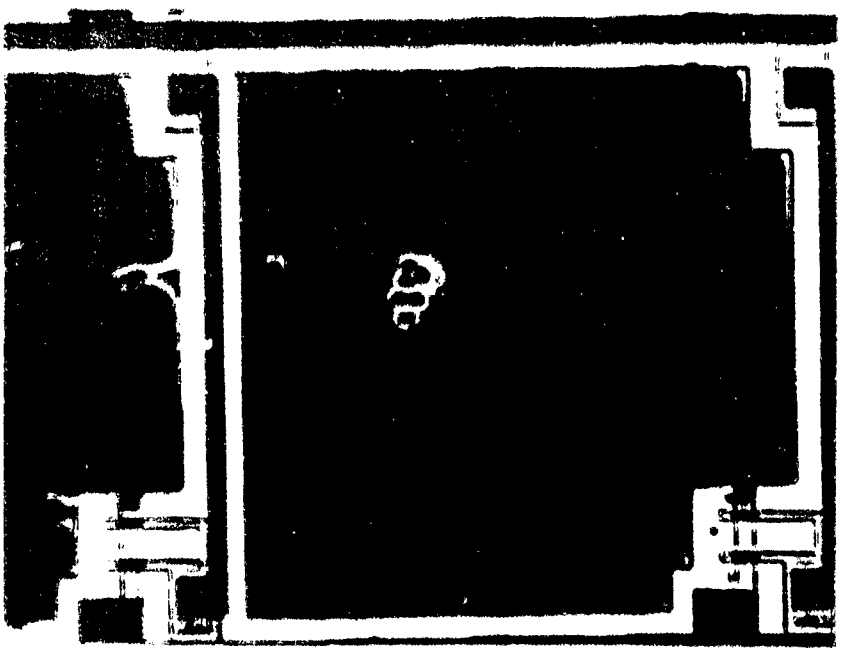


Figure 3 *Photograph of Fully Functional Transfer AMLCD Assembled with Color Filters Center. The Measured Contrast Ratio is Approximately 60:1*



Non-
Transferred
Display



Transferred
Display

Figure 38 *Photomicrograph of Individual Pixel Electrodes of a Poly Display (Upper Figure) and Transfer Silicon Display (Lower Figure) Showing Absence of Disclinations in the Transferred Display.*

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